

Intel(R) E7501 High Performance Appliance
Platform - Intel(R) Xeon(tm) Processor
FAB C Rev B V1.0

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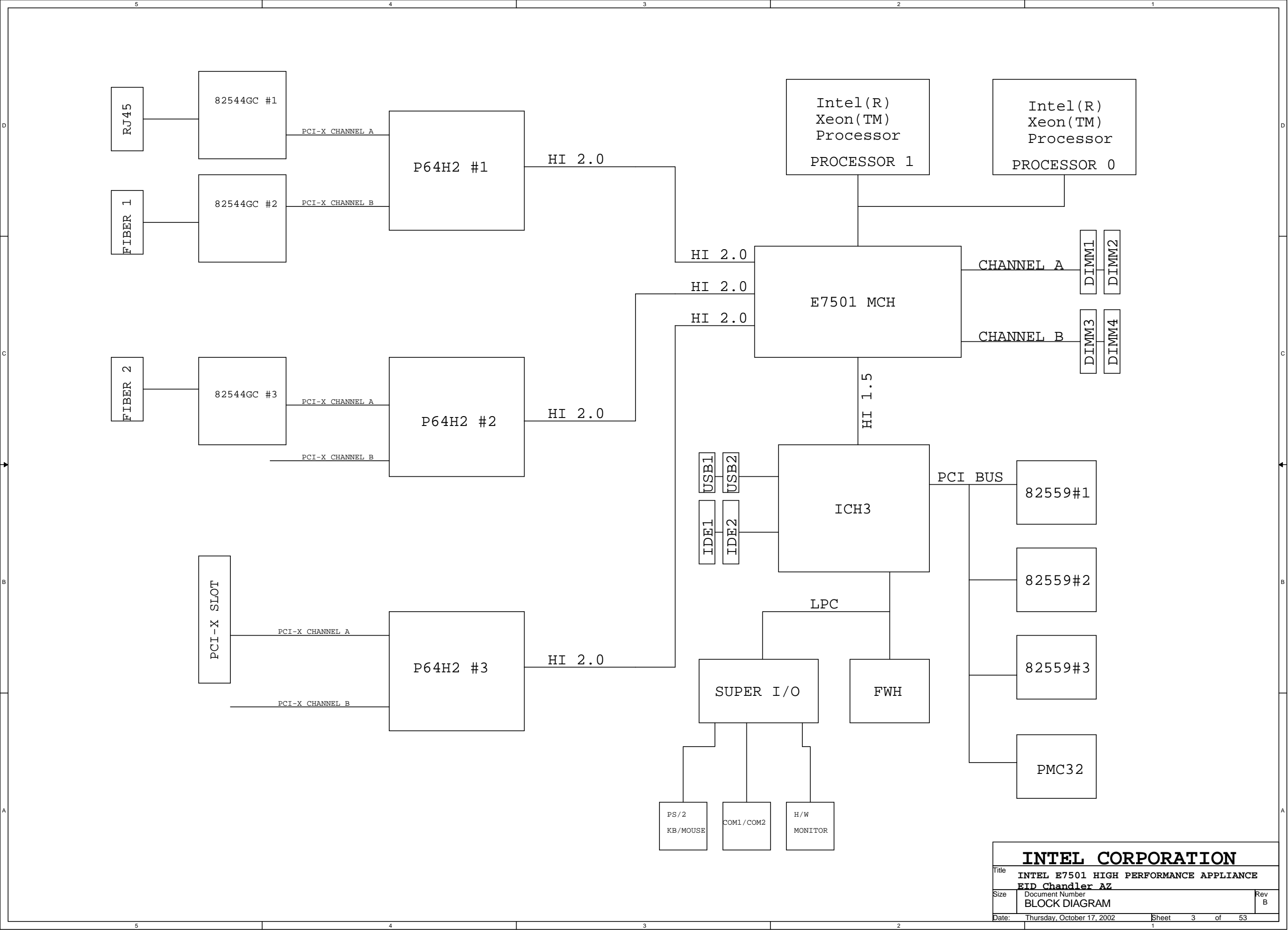
Revision	Changes
Fab A	Initial Version DUAL Planar Mezzanine Boards
Fab B	1. Combine System board and I/O board Removing original MICTOR connectors 2. Add the circuit for Fiber errata 3. Add two copper Gigabit for Fiber/Copper flexible design. 4. Adjust the resistors/capacitors value to meet Intel reference schmatic.
Fab C	1. Add more caps on MCH 2.5V

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FAB C Rev B V1.0

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<div>1. CLK</div> <div>a. HOST_CLK : refer to P38 of D.G., Rout the CPU CLK differentially.</div> <div>b. CLK66: refer to P42 of D.G., there is no connector between MCH and P64H2 , so the CLK66 to P64H2 should be 0.34" shorter than the CLK66 to MCH.</div> <div>c. CLK33: refer to P45 of D.G. , CLK33_ICH3 should be matched to +-100mils of CLK66. and the CLK33 to the on board PCI device should be length matched to CLK33_ICH3.</div> <div>d. CLK14 and USBCLK : refer to P48 of D.G.</div> <div>e. CLOCK Driver Decoupling : refet to P50 of D.G.</div> <div>2. System Bus Routing Guidelines</div> <div>a. refer to P53 of D.G.</div> <div>b. Trace width/spacing : 5/15 mils, serpentine ratio of 5:1</div> <div>c. 2X and 4X signal group: MCH to Processor -> 3.0"-6.5" pin to pin, Processor to Processor -> 3.0"-7.0" pin to pin. Total bus length must not exceed 13.5". Balance trace lengths +- 25 mils with respect to the associated strobes between agent to compensate for the stub creates by th processor package. Route all signals within the same strobe group on the same layer for the entire lenth of bus. Never change layers on 2X and 4X signals. Never route over a plane split.</div> <div>d. DSTBN[3:0]#/DSTBP[3:0]# and ADSTB[1:0]#: Follow the same routing rule asthe 2X and 4X Signal Group. Maintain a 25 miil spacing around each strobe signals. Never route over a plane split.</div> <div>e.Common Clock Signal: Follow the same routing rules as the 2X and 4X Signal Group, however no length compensation is necessary. If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.</div> <div>f. Topology: Daisy chain with the chipset at one end of the system bus and Processor 0 at the other. End processor must have on-die termination enabled.</div> <div>g.Routing Requirements: No motherboard contribution to stub length of middle processor (35 mil max trace via to pad). Stripline, ground referenced only.</div> <div>h. Motherboard Impedance: 50 ohm</div> <div>3. Memory Interface Routing Guidelines</div> <div>a. Source Synchronous Signals : DQS[17:0], DQ[63:0], CB[7:0]. Command Clocks: CMDCLK[3:0], CMDCLK[3:0]# Source Clocked Signals: MA[12:0], RAS#, CAS#, WE#, BA[1:0]. Chip Selects: CS#[7:0]. Clock enable: CKE</div> <div>b. Source Synchronous Signal Group Routing: refer to P78 of D.G. use 33 ohm for E7500, or 39 ohm for E7501.</div> <div>c. Command Clock Routing: refer to P81of D.G. , Route the clock differentially.</div> <div>d. Source Clocked Signal Group Routing: refer to P83 of D.G. use 33 ohm terminator for E7500 or 39 ohm for E7501</div> <div>e. Chip Select Routing: refer to P84 of D.G. , use 33 ohm terminator for E7500 or 39 ohm for E7501. length matched to Command Clock length +- 875 mils.</div> <div>f. Clock Enable Routing: refer to P85 of D.G. , 40 ohm impedance, 33 ohm terminator for E7500 or 39 ohm for E7501.</div> <div>g. Receive Enable Signal: refer to P87 of D.G. , Total length is 15" +- 100 mils.</div> <div>h. DDR Signal Termination: refer to P92 of D.G.</div> <div>i. Decoupling Requirements: refer to P93 of D.G.</div> <div>4. Hub Interface</div> <div>a. Common Clock Signals : HI[19:16]_x Source Synchronous Signals : HI[21:20]_x, HI[15:0]_x, PSTRB, PSTRBS, PUSTRB, PUSTRBS Miscellaneous Signals : HIRCOMP_x, HISWING_x, HIVREF_x</div> <div>b. refer to P95 of D.G. , the same data group must be length matched within 0.25", the same strobe pair is also length matched with 0.25". and the longer signal of strobe pair must have the same length as the longest signal of data group.</div> <div>c. HIRCOMP pull high resistor must be put within 1 inch of MCH</div>				
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<div>5. P64H2 & PCI-X Bus</div> <div>a. Design rule can refer to P105 of D.G.</div> <div>b. Timing Crititical Signal : PxAD[63:0], PxC/BE#[7:0], PxDEVSEL#, PxPERR#, PxSERR#, PxREQ[5:0]#, PxPLOCK#, PxPAR64.</div> <div>Non-Timing Critical Signals: PxGNT[5:0]#, PCIXCAP, Px_133EN, PxREQ64#, PxACK64#, PxIRQ[15:0]</div> <div>c. Route the signals stripline with 5-mil trace width with 10 mil spacing, with impedance 50 ohm</div> <div>d. Must meet Clock configuration no matter PCI-X slot or on board Gigabit Lan. refer to P111 of D.G.</div> <div>6.Copper Gigabit</div> <div>a. Transmission line design rule from 544GC to RJ45,differential impedance is 100 ohm</div> <div>b. The lengths of the differential traces (within each pair) should be equal within 50 mils and as symmetrical as possible.</div> <div>c. To reduce crosstalk interference on signals between pairs, the minimum distance between unlike differential pairs must be 50 mils.</div> <div>d. To minimize impedance discontinuity, traces within differential pairs must not have bends over 45 degrees.</div> <div>e. To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 300 mils of the differential pairs.</div> <div>f. The four differential pairs are terminated with 49.9 ohm resistors, placed near the 82544GC. Be sure to layout symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.</div>				
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CONNECTOR:

J1: 10/100/1000 bits RJ45
J2: 10/100/1000 bits RJ45
J3: 10/100/1000 bits RJ45
J4: 10/100M Bits RJ45
J5: 10/100M Bits RJ45
J6: 10/100M Bits RJ45
J7: PS/2 KB/MOUSE
J8: COM1
J9: USB
J10: FWH Debug Connector
J11: Fiber Gigabit
J12: Fiber Gigabit
J13: Hook for MCH Heat Sink
J14: Hook for MCH Heat Sink
J15: PCI-X Slot
J16: Hook for MCH Heat Sink
J17: Hook for MCH Heat Sink
J18: ITP PORT
J19: Connector for LEDs, RESET Button, POWER Button
J21: COM2 for LCD Panel
IDE1: SECONDARY IDE CONNECTOR
IDE2: PRIMARY IDE CONNECTOR
ATX1: ATX POWER CONNECTOR
CPUFAN1: CPU FAN POWER CONNECTOR
CPUFAN2: CPU FAN POWER CONNECTOR
SYSFAN1: SYSTEM FAN POWER CONNECTOR
SYSFAN2: SYSTEM FAN POWER CONNECTOR

INTERRUPT ROUTING TABLE:

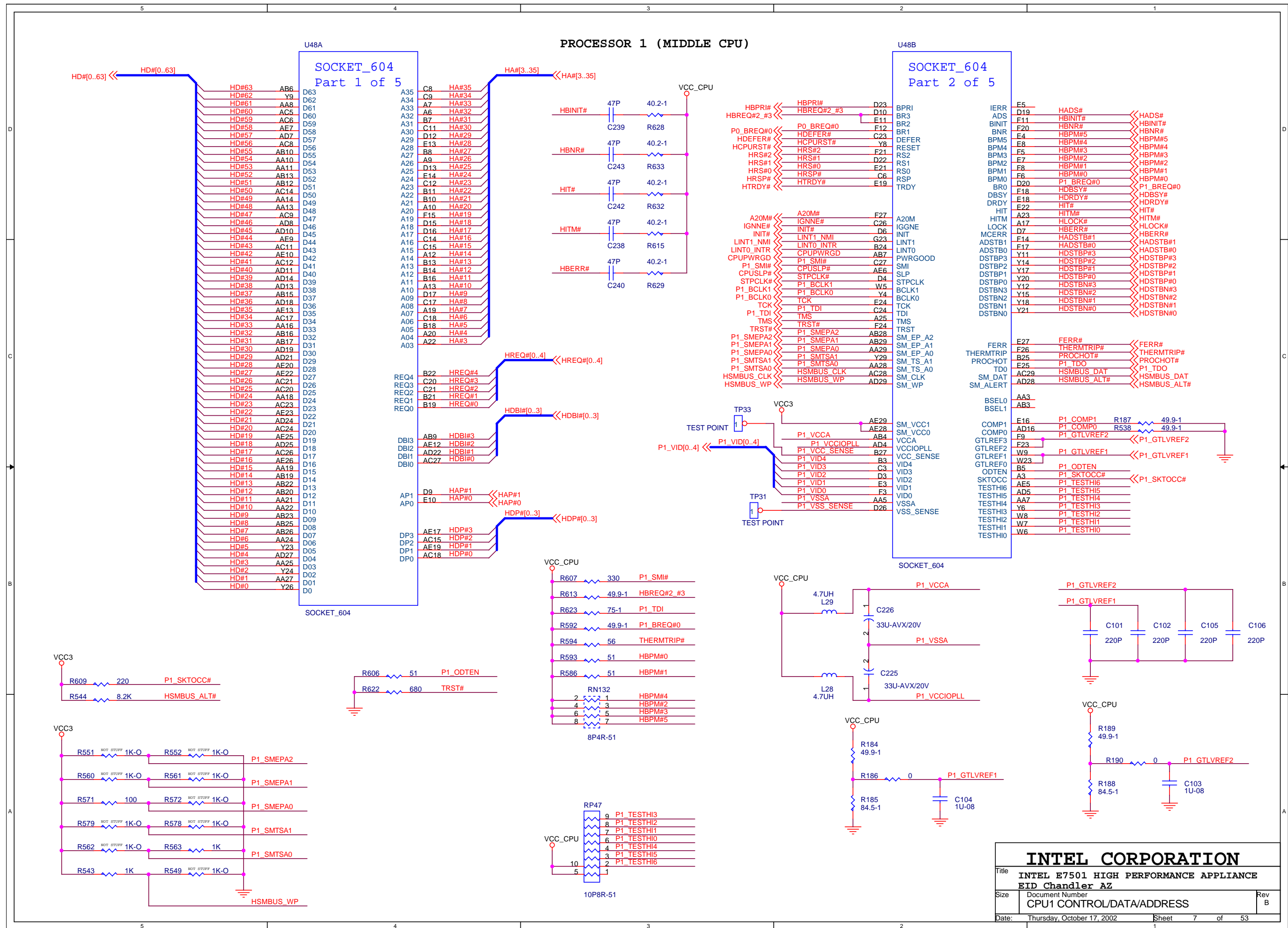
ICH3 INTERRUPT: P64H2#1
PIRQA#: P64H2#1 P1AIRQ0: 82544GC#1 FOR COPPER
PIRQB#: P64H2#2 P1BIRQ0: 82544GC#2 FOR FIBER
PIRQC#: P64H2#3
PIRQD#: NO USE
PIRQE#: 82559#1
PIRQF#: 82559#2
PIRQG#: 82559#3
PIRQH#: NO USE

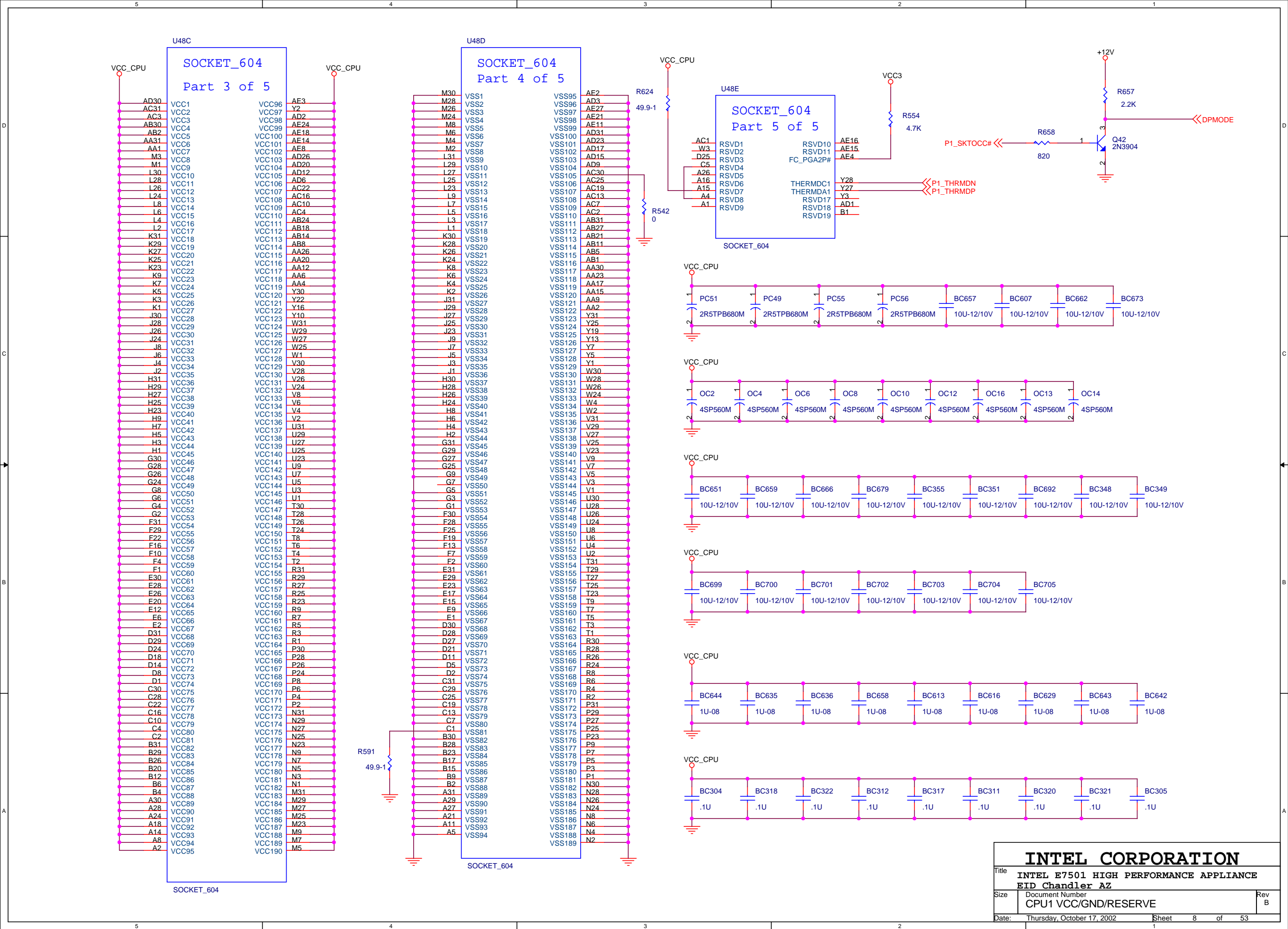
GPIO FOR LEDS

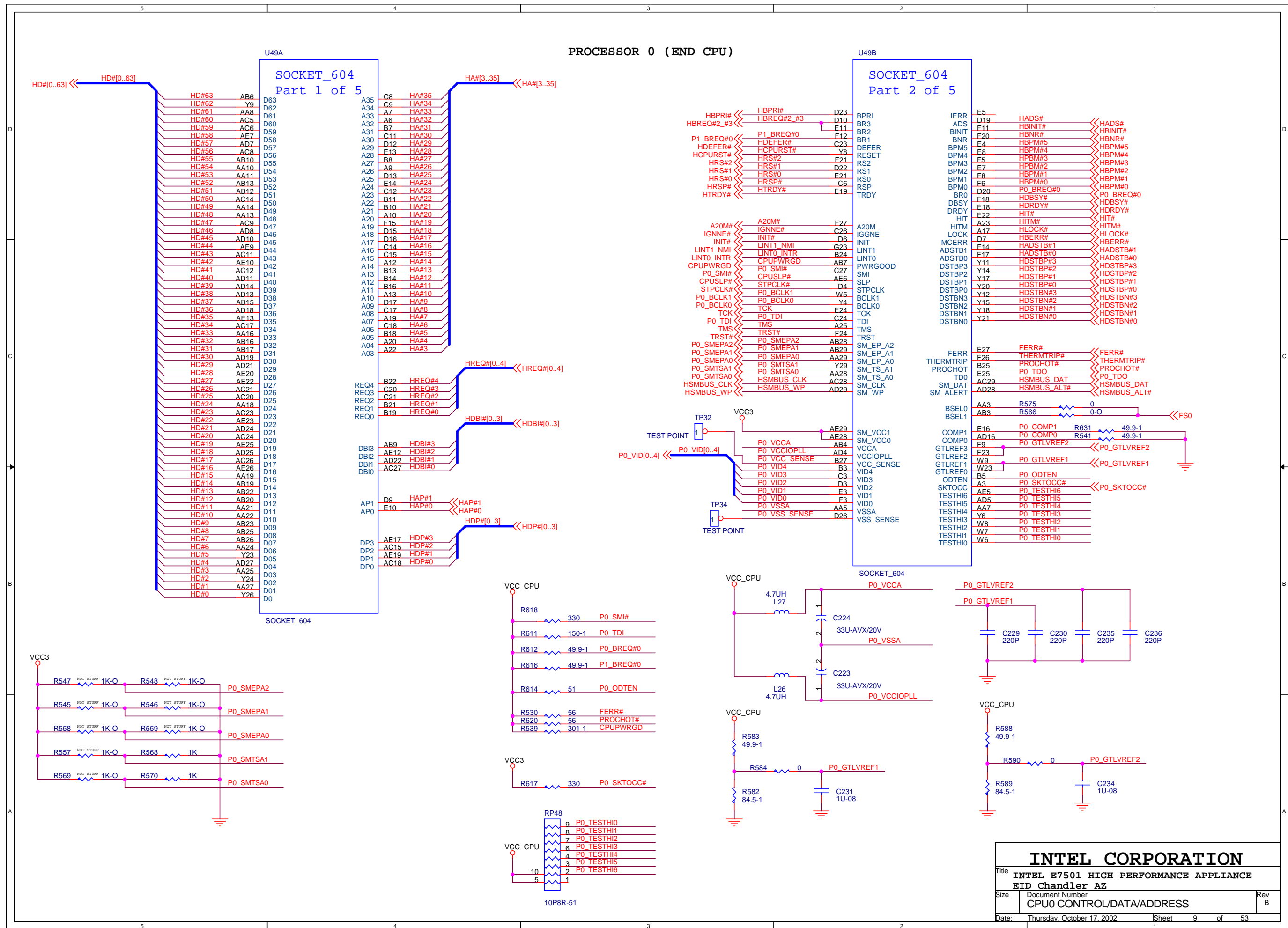
GPIO34: LED CONTROL FOR POWER LED
GPIO35: LED CONTROL FOR CPU OVER HEAT LED
GPIO36: LED CONTROL FOR PRIMARY HDD LED
GPIO37: LED CONTROL FOR SECONDARY HDD LED
GPIO38: LED CONTROL FOR 10/100M BIT PORT1 ACTIVITY LED
GPIO39: LED CONTROL FOR 10/100M BIT PORT2 ACTIVITY LED
GPIO40: LED CONTROL FOR 10/100M BIT PORT3 ACTIVITY LED
GPIO41: LED CONTROL FOR GIGABIT PORT1 ACTIVITY LED
GPIO42: LED CONTROL FOR GIGABIT PORT2 ACTIVITY LED
GPIO43: LED CONTROL FOR GIGABIT PORT3 ACTIVITY LED

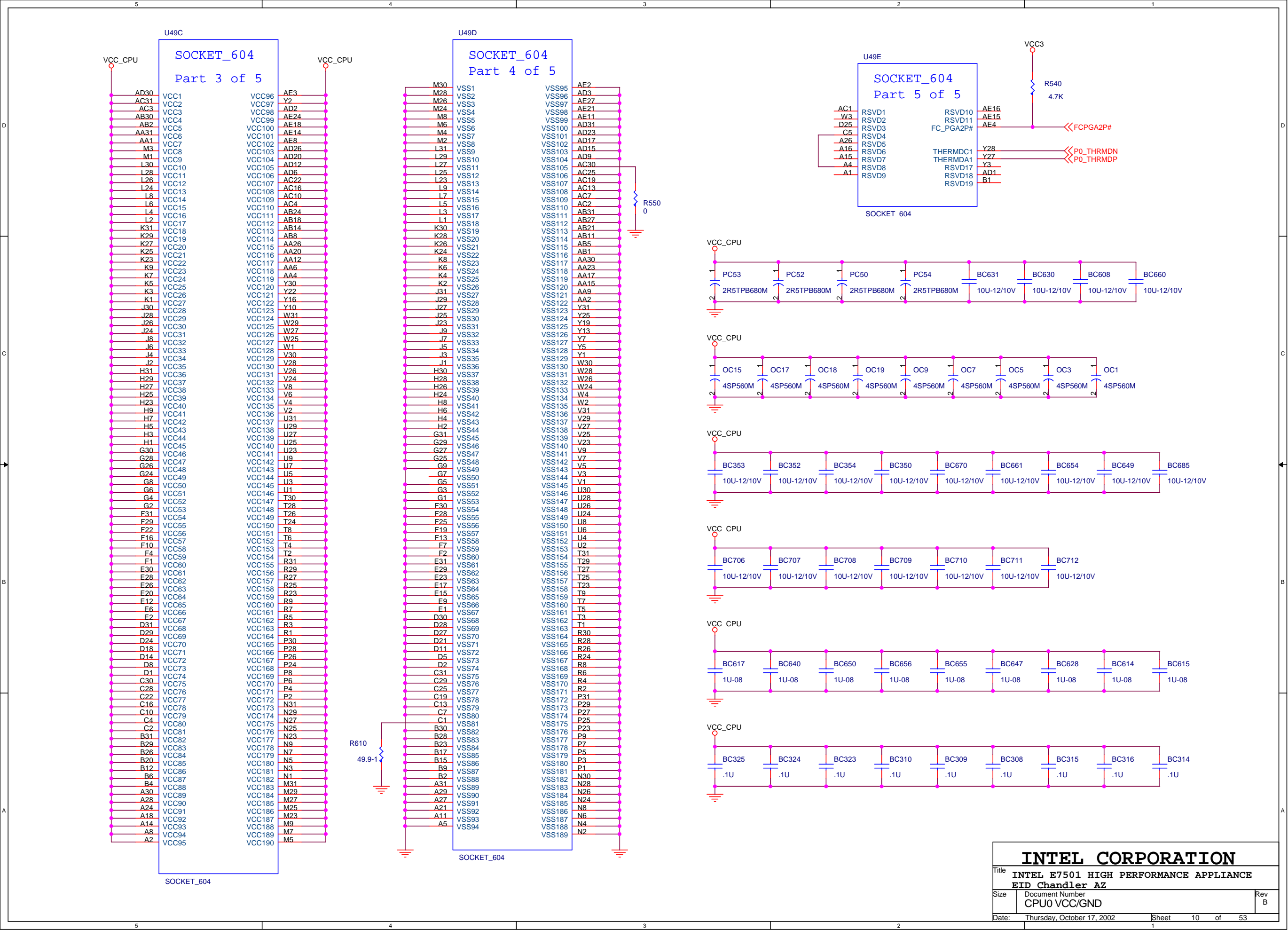
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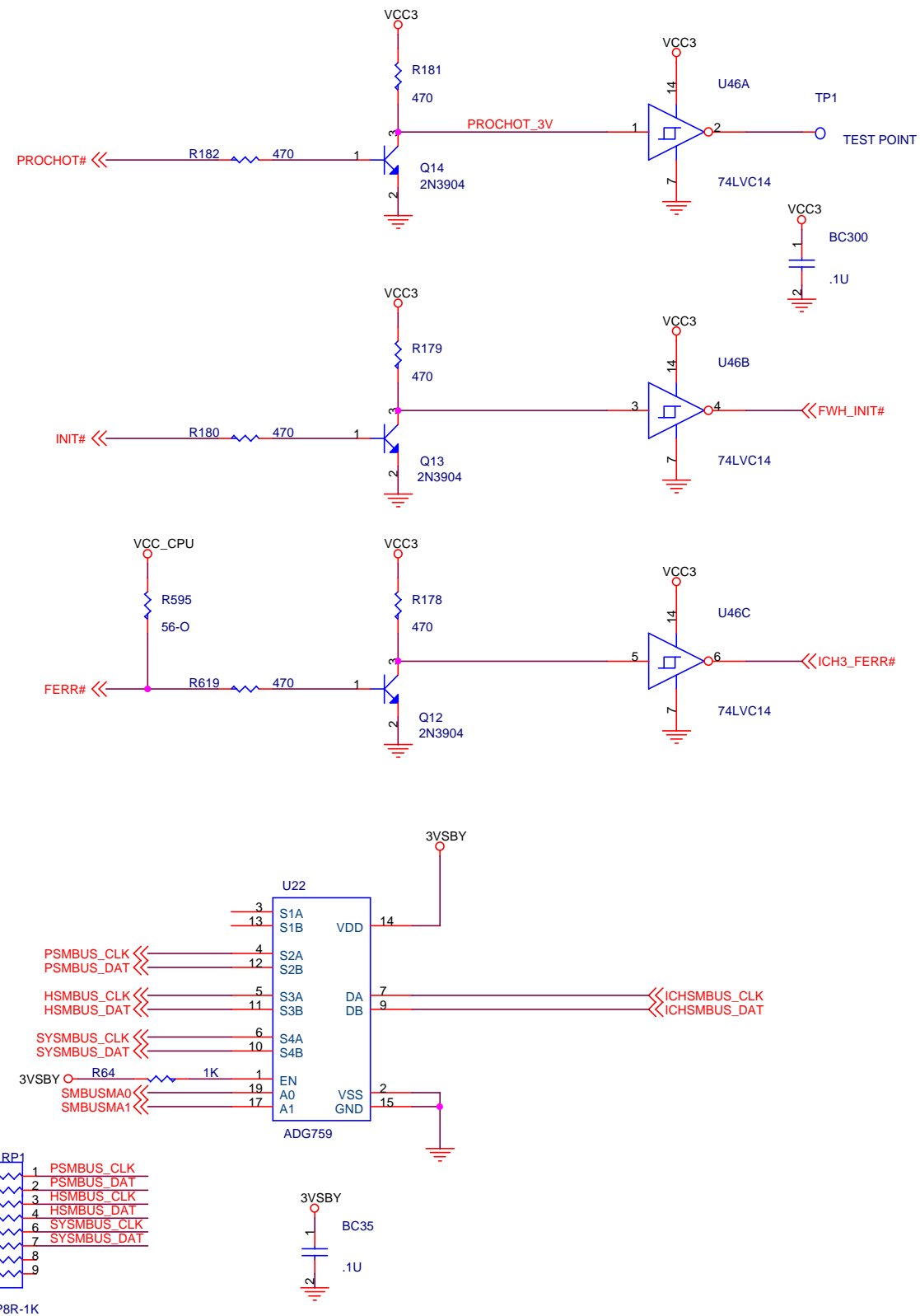
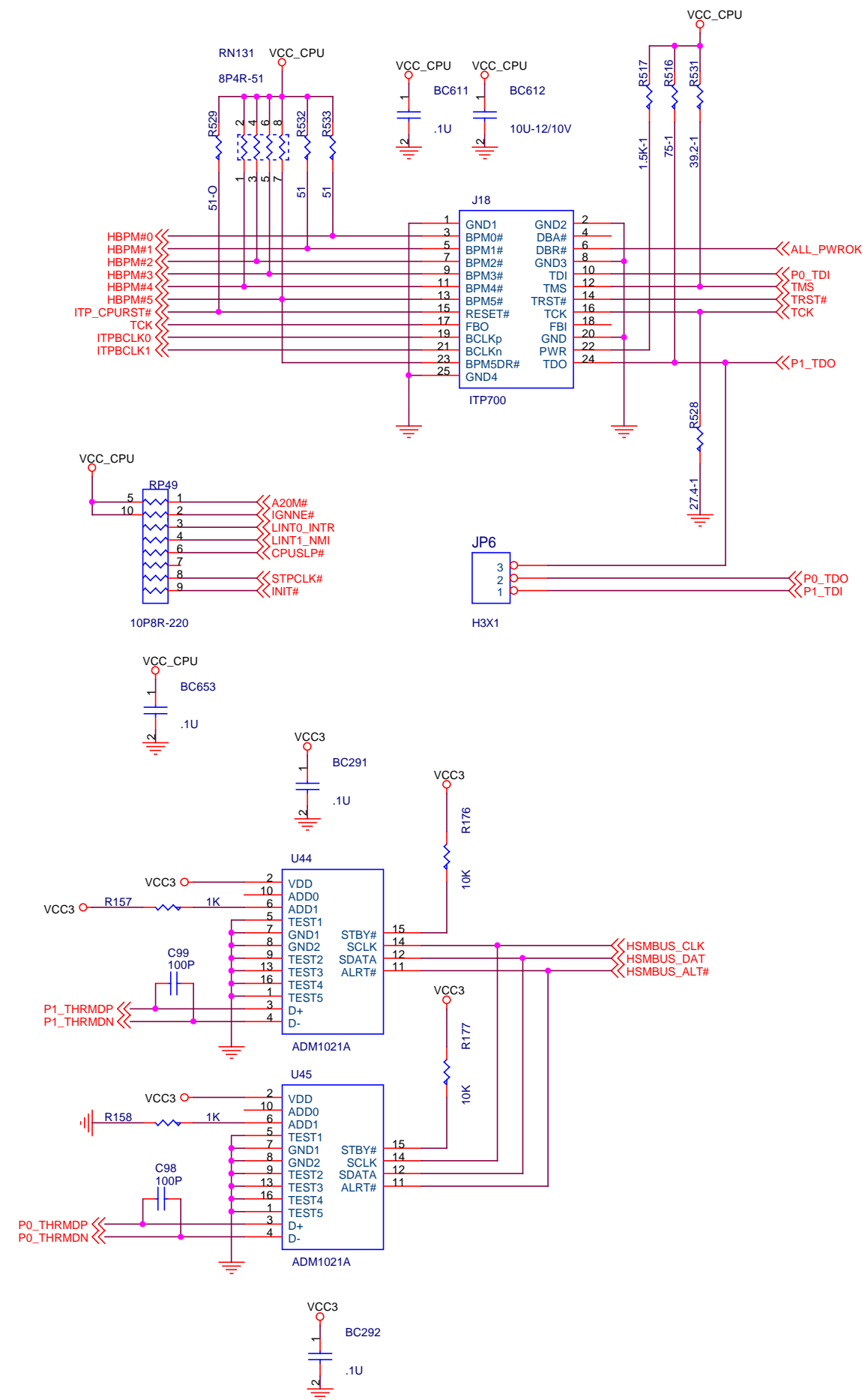
JP1: BUZZER
ON ENABLE
OFF DISABLE
JP2: TCO TIMER
ON DISABLE
OFF ENABLE
JP3: BIOS WRITE PROTECT
ON WRITE ENABLE
OFF WRITE PROTECT
JP4: CPU SAFE MODE
ON ENABLE
OFF DISABLE
JP5: CMOS CLEAR
1-2 NORMAL
2-3 CLEAR
JP6: ITP PORT
1-2 DP
2-3 UP
JP7: VRM
1-2 DEFAULT
JP8: VRM VID SETTING
JP9: FAN POWER
1-2 +12V
2-3 5V

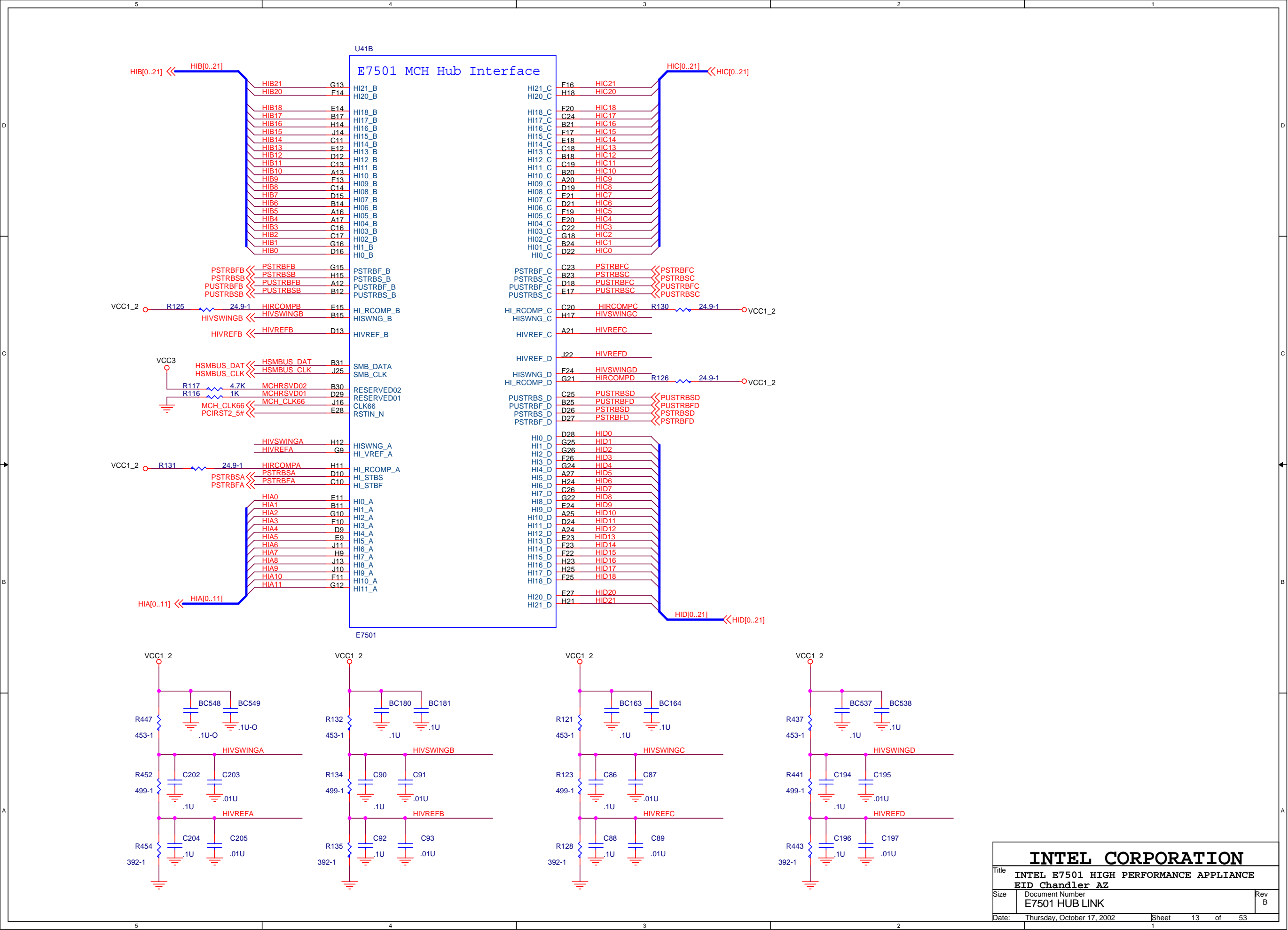


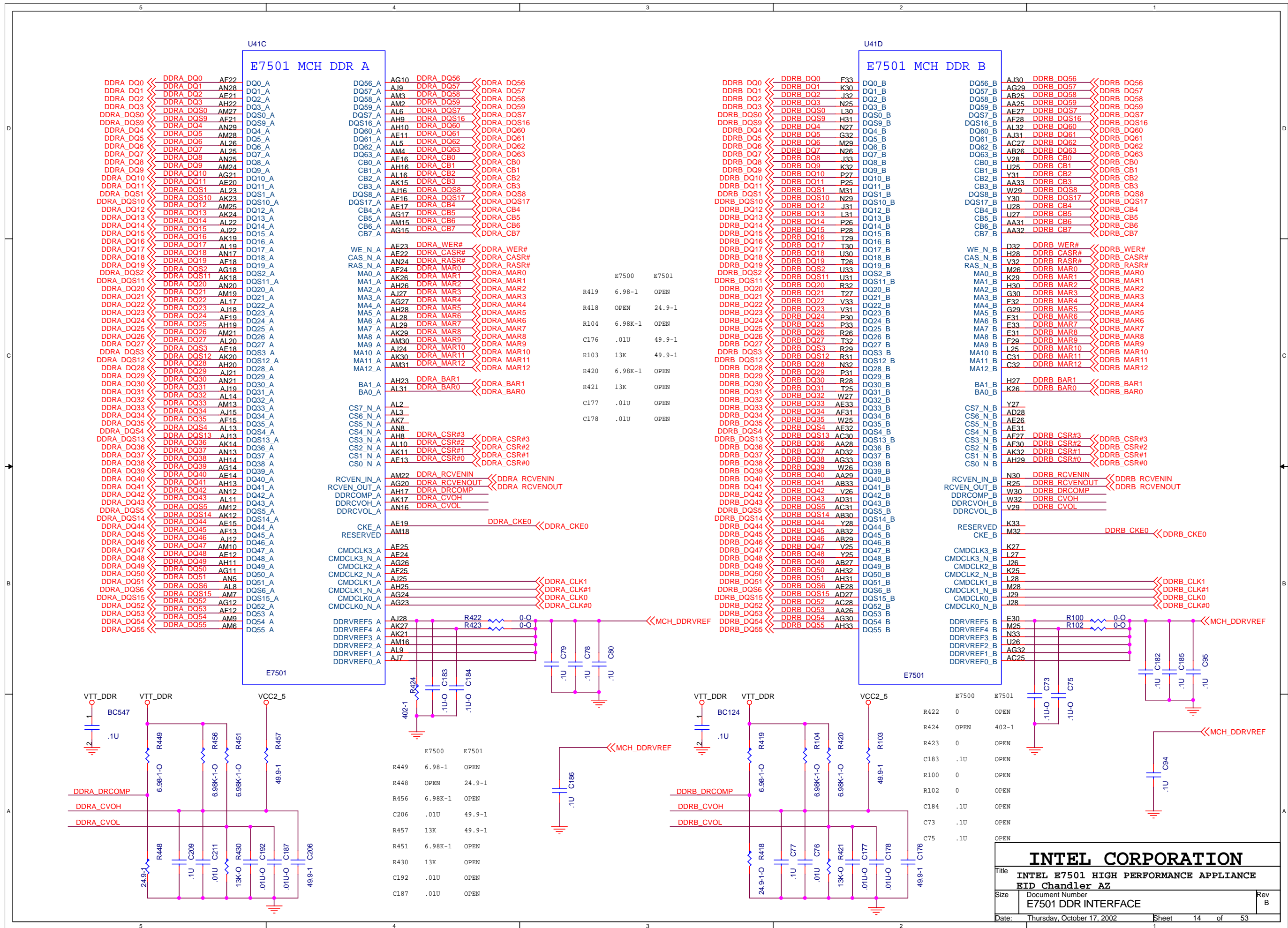


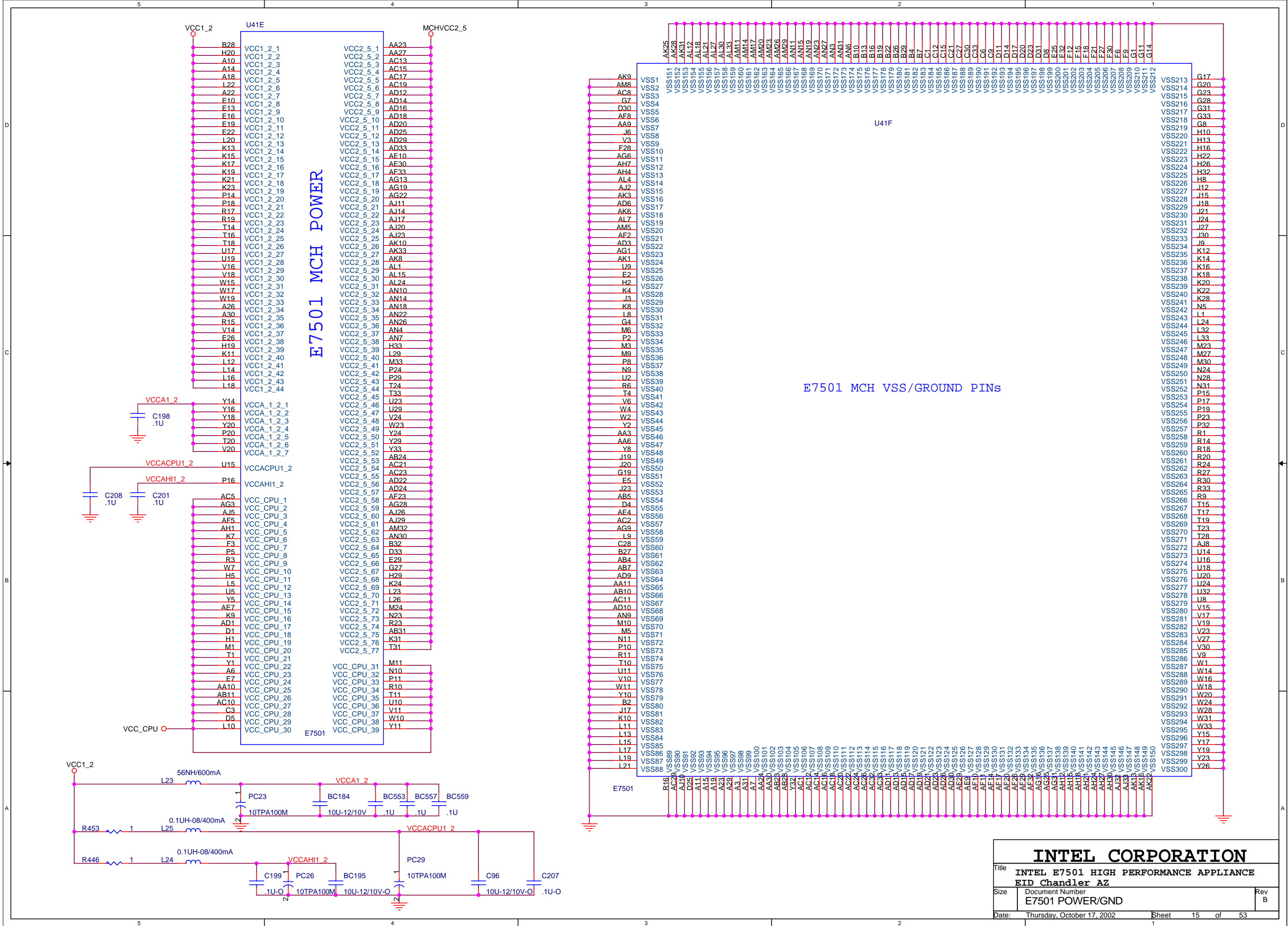


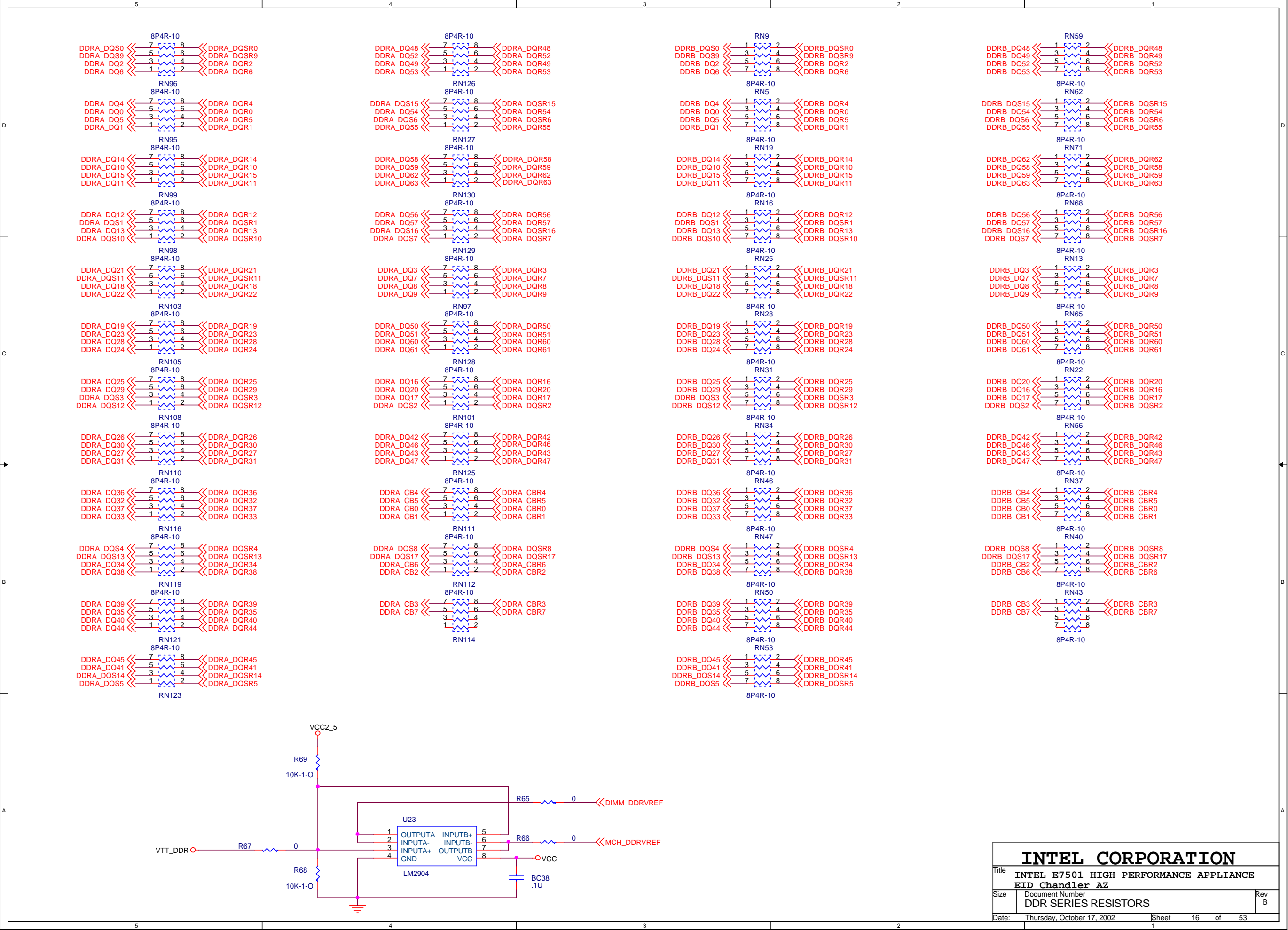












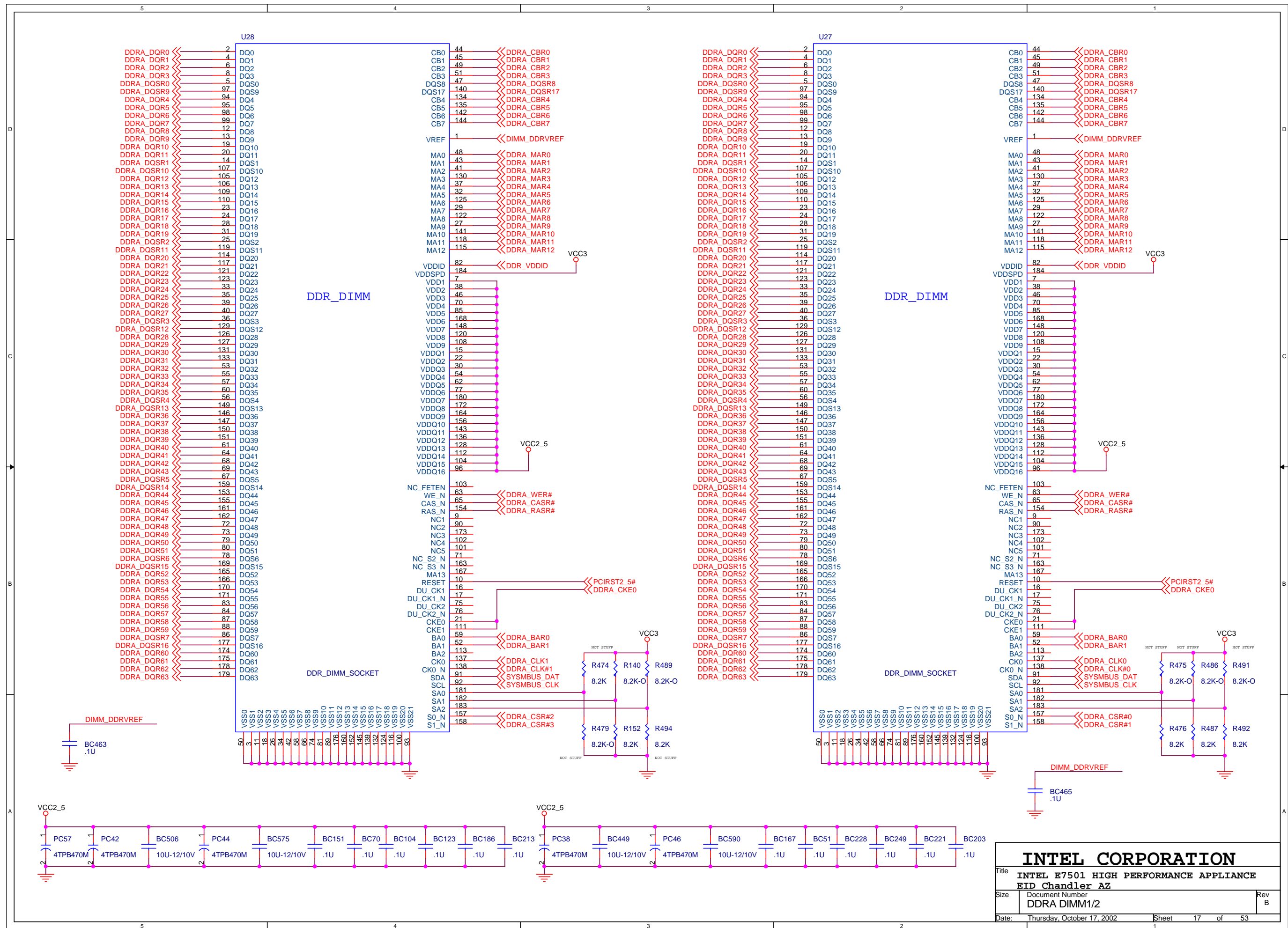
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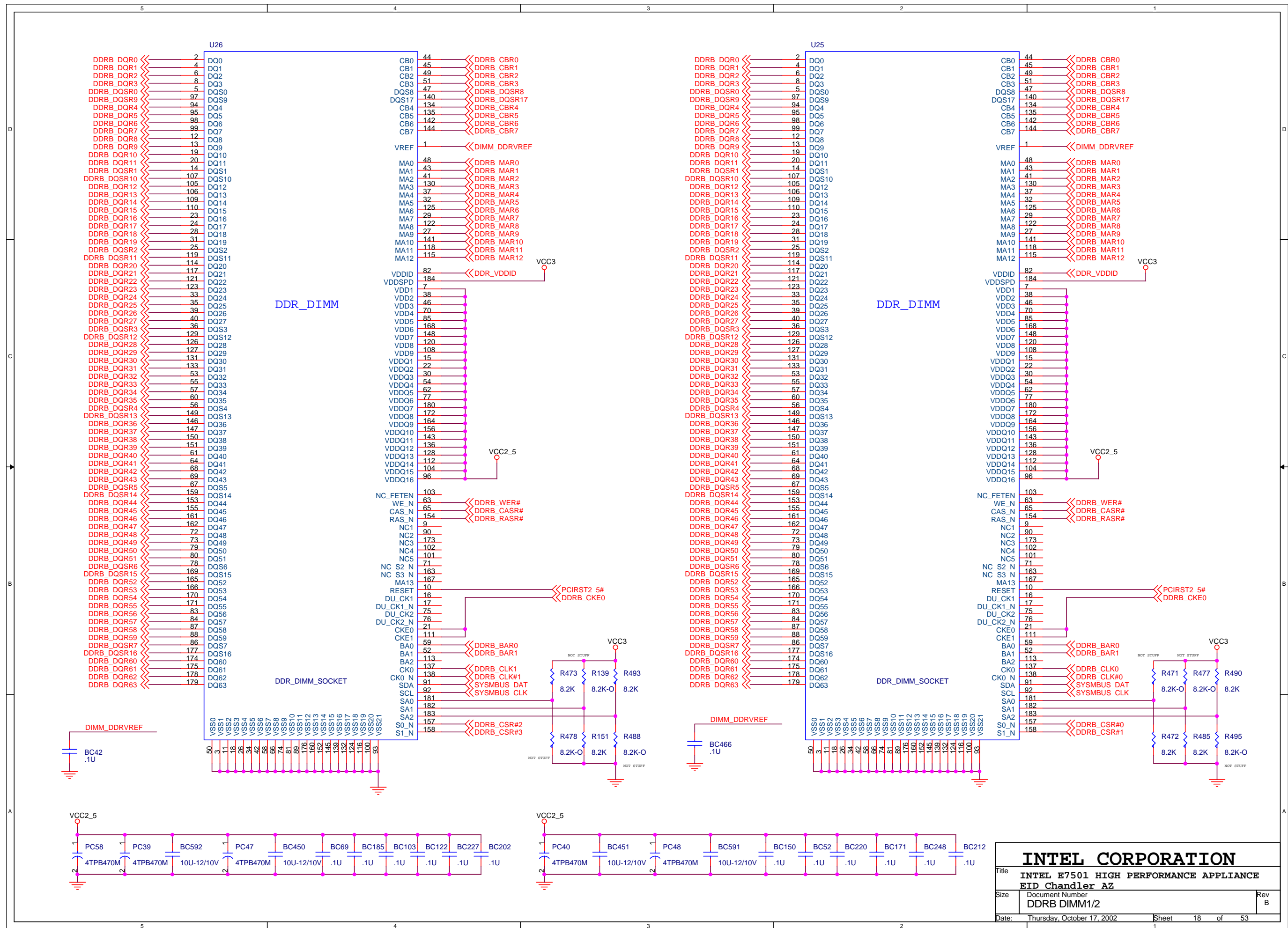
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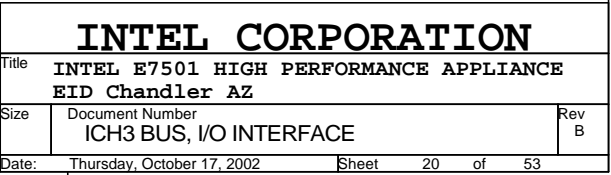
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DDR SERIES RESISTORS

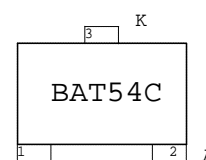
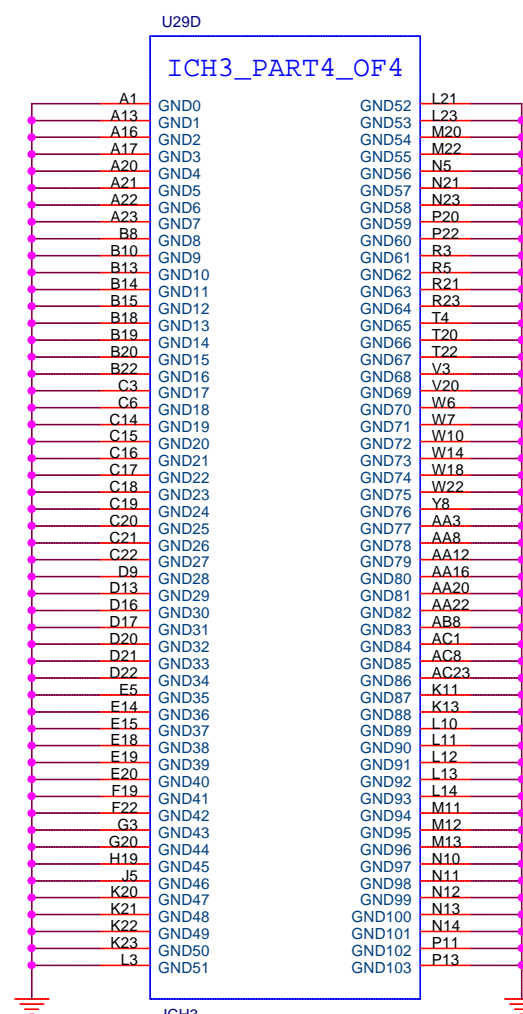
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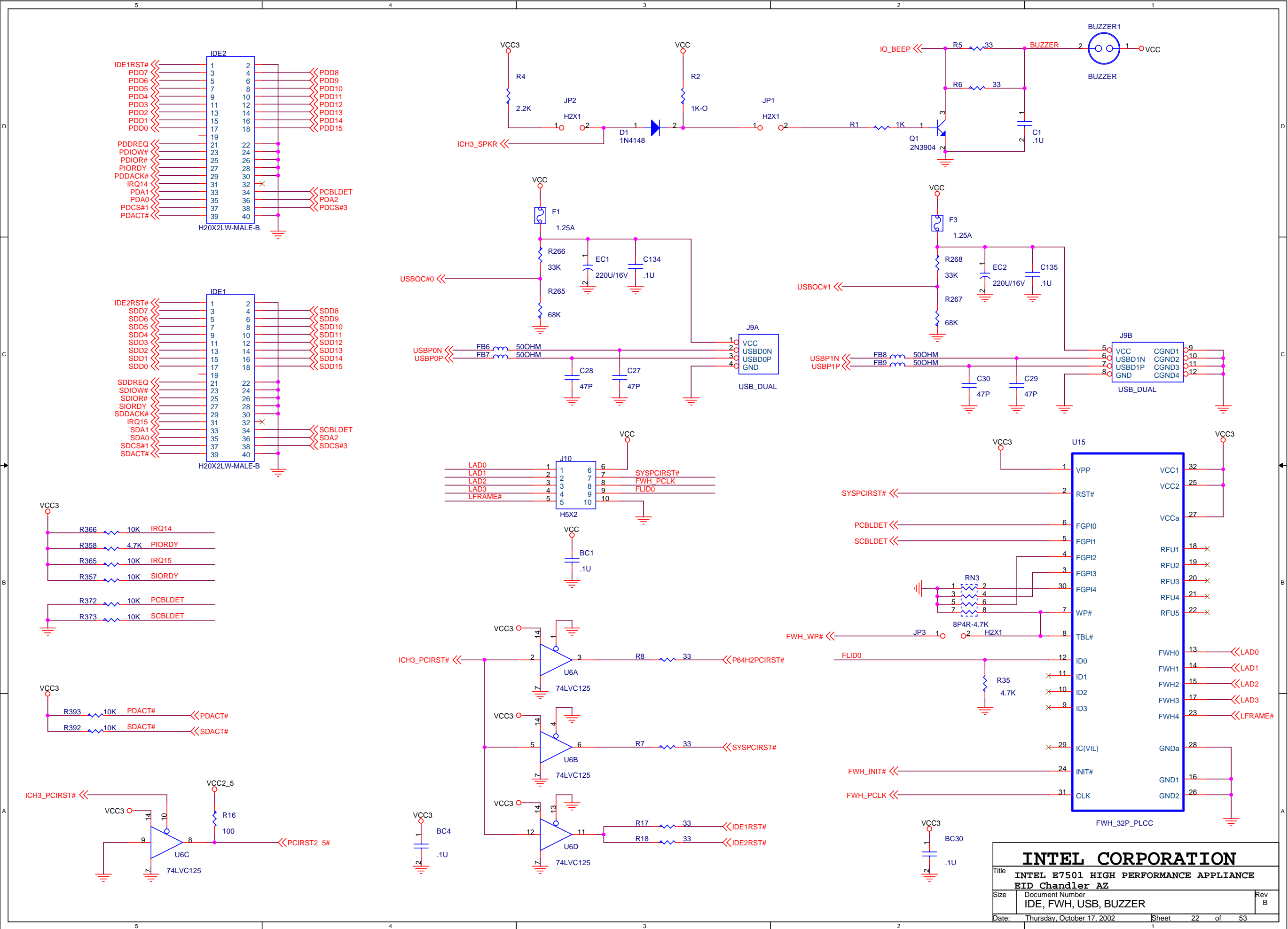
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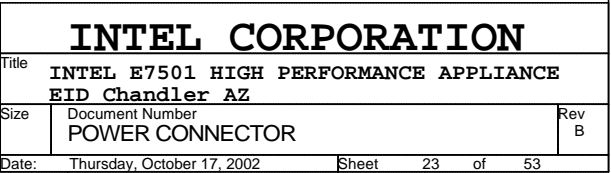


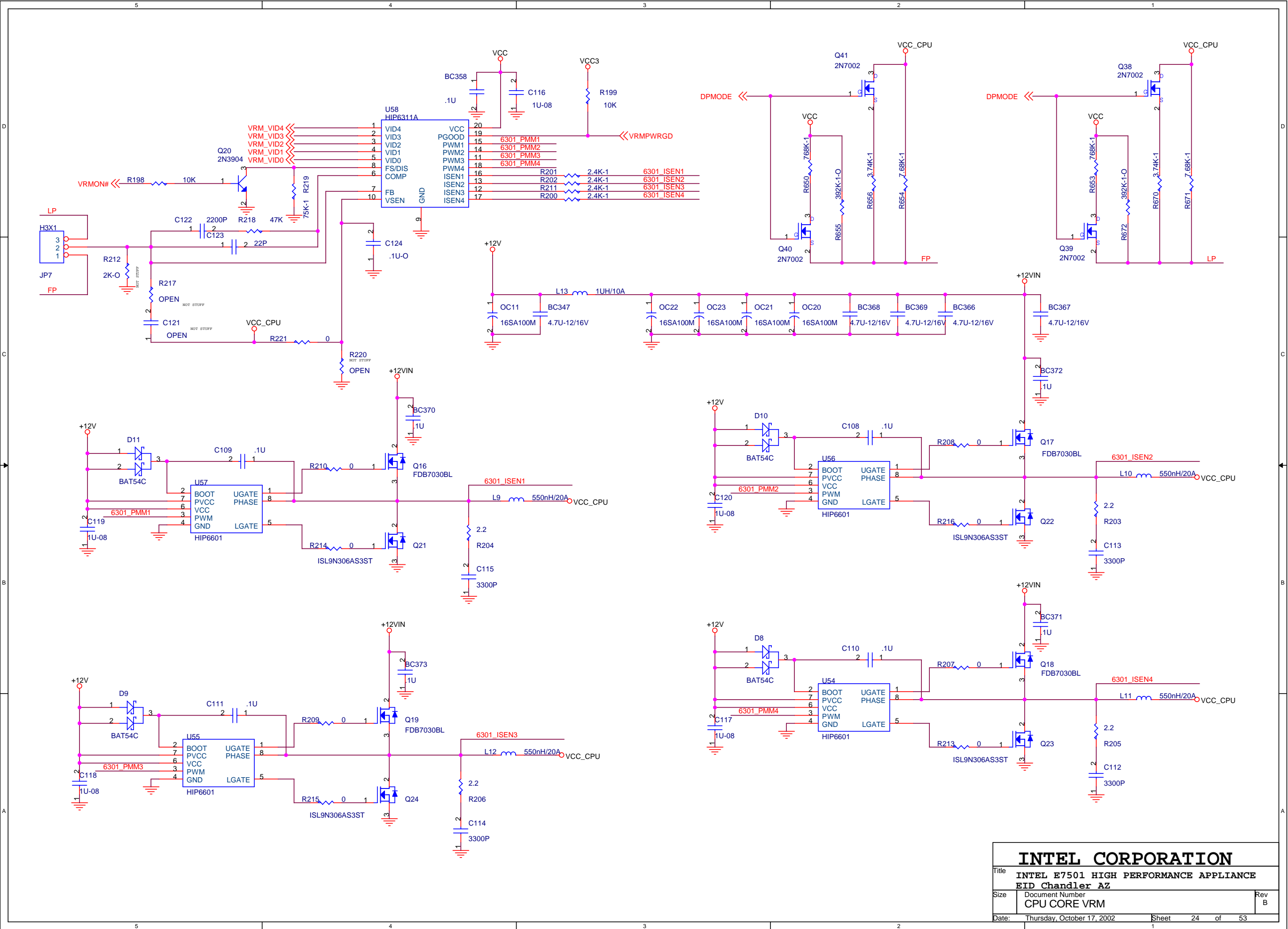


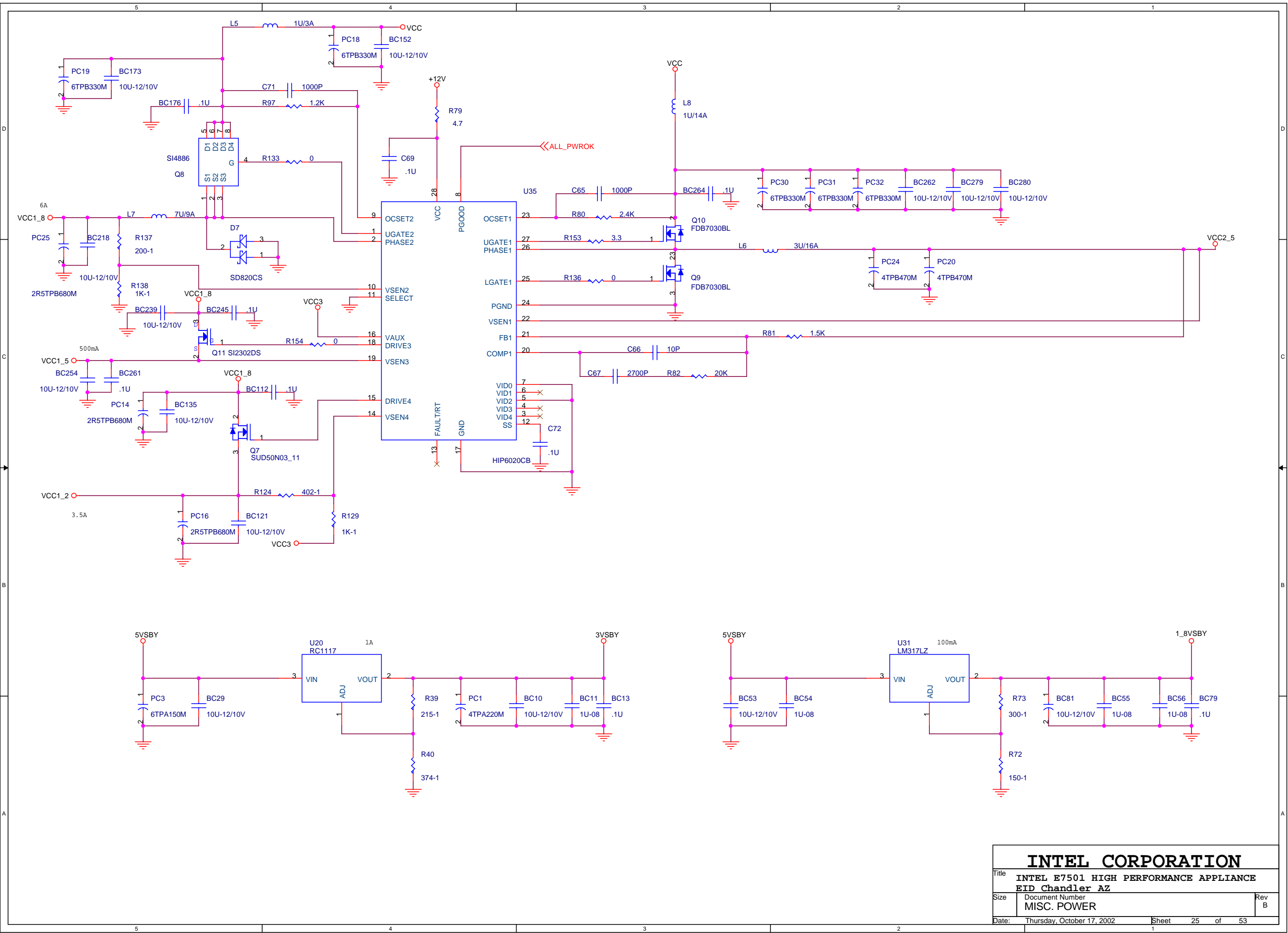


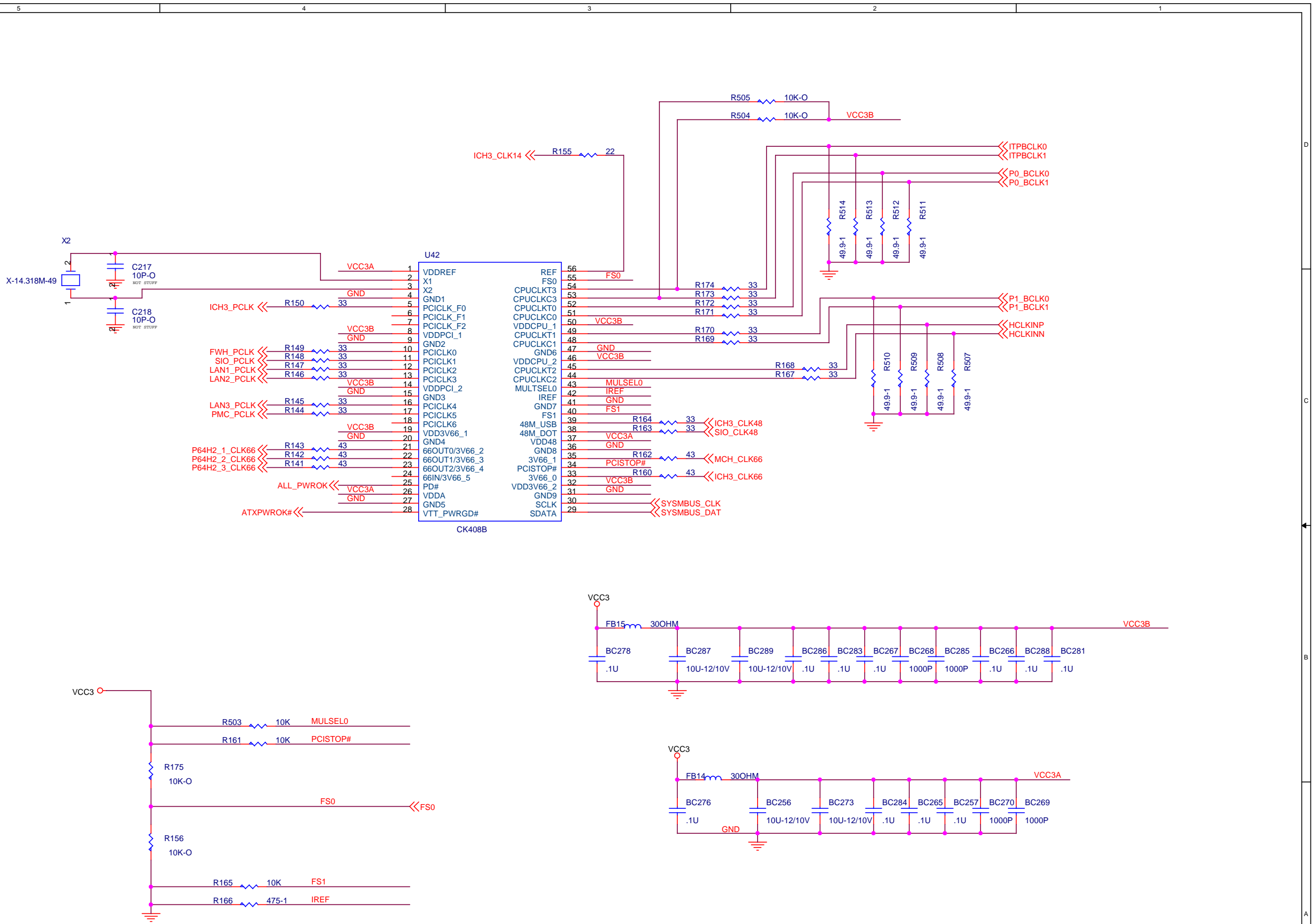


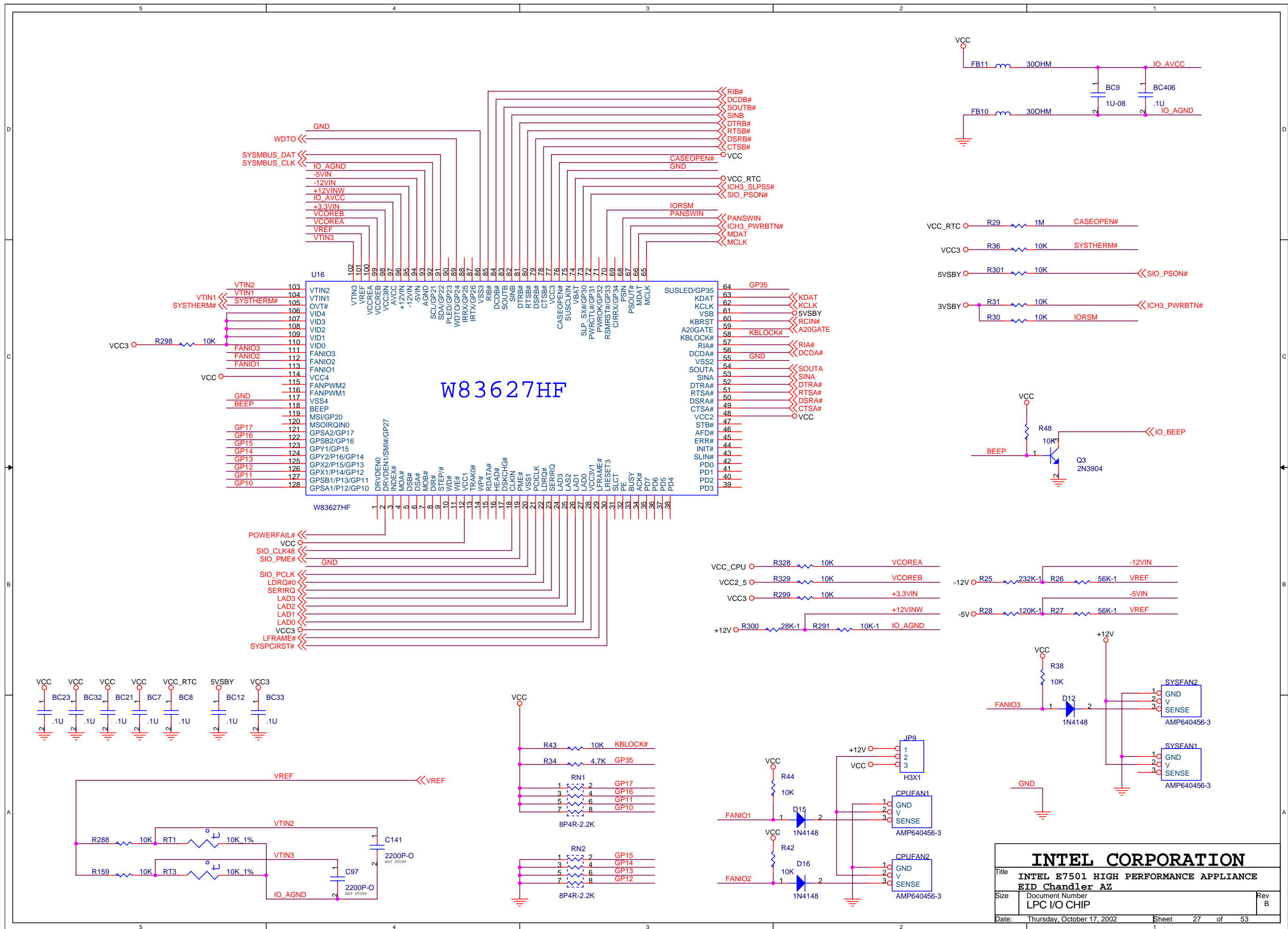


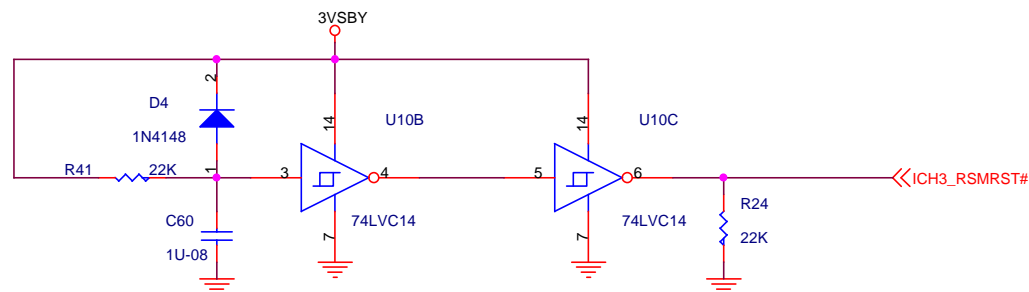
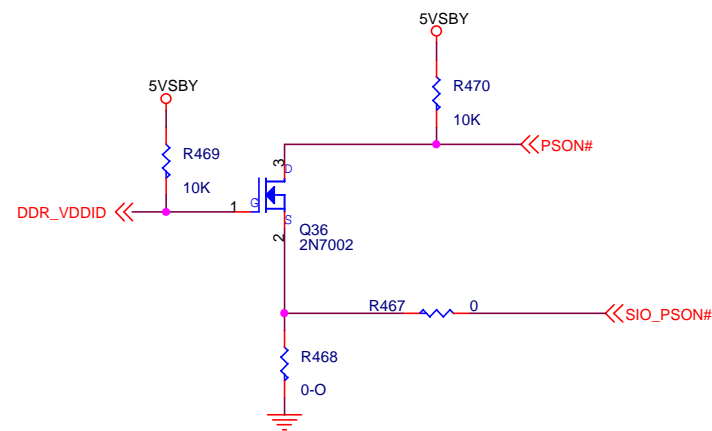
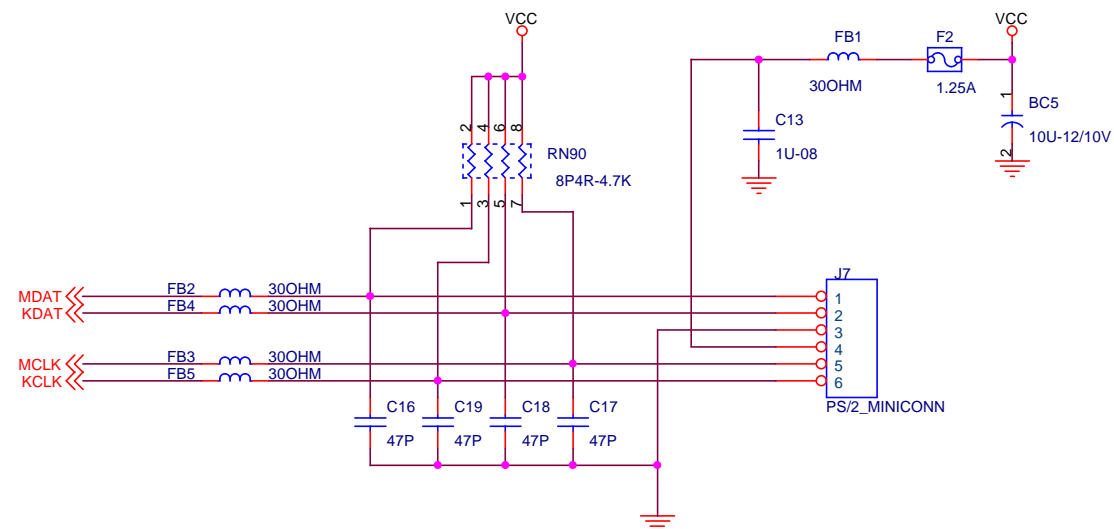
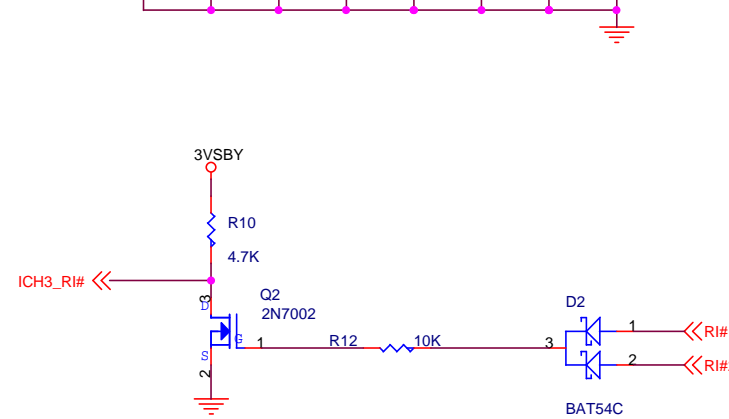
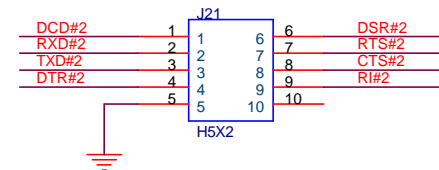
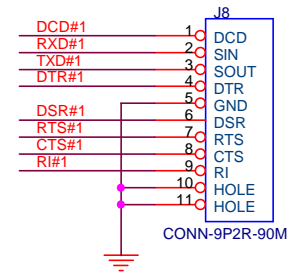


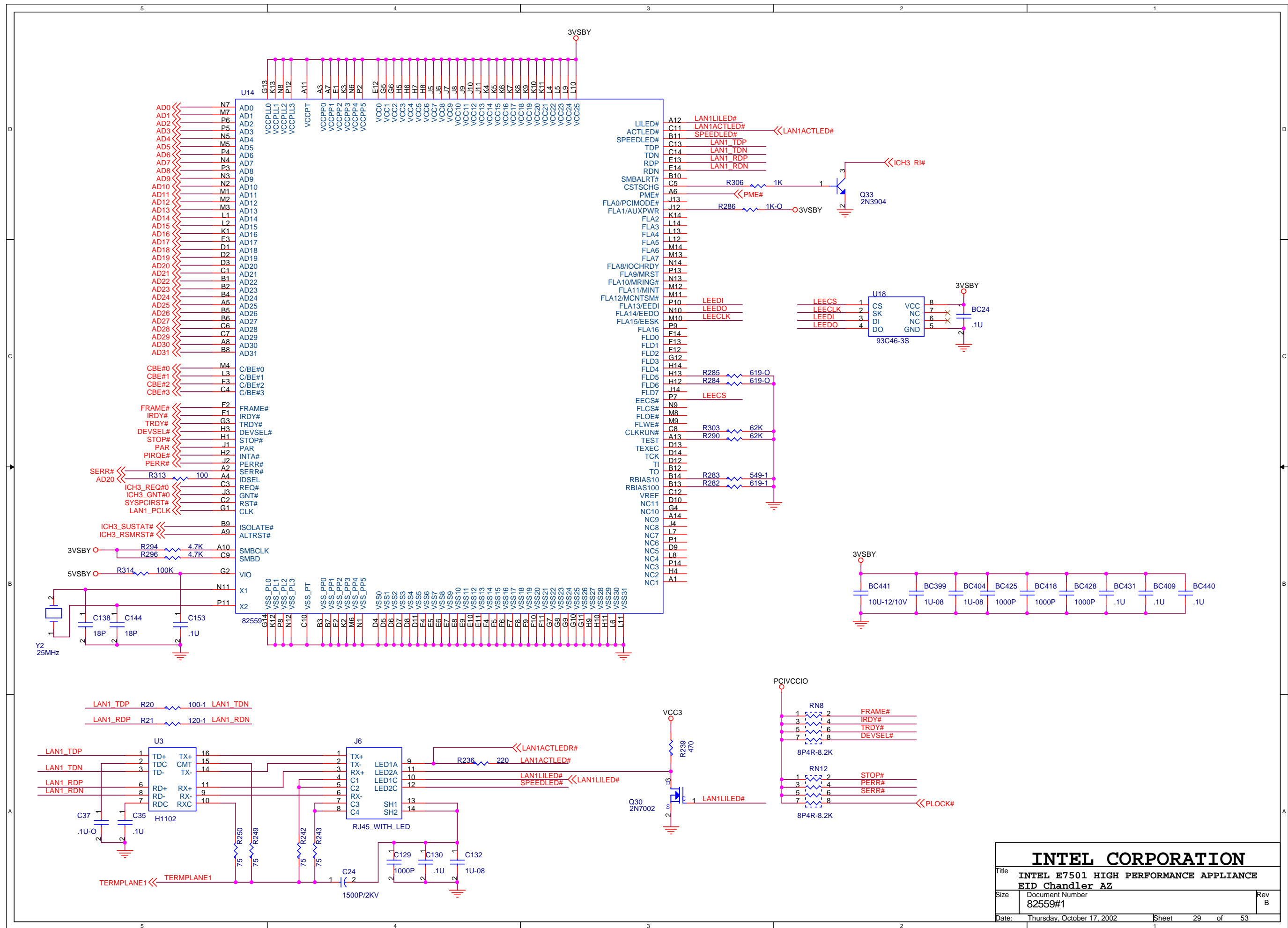


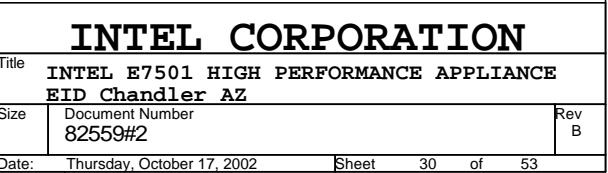


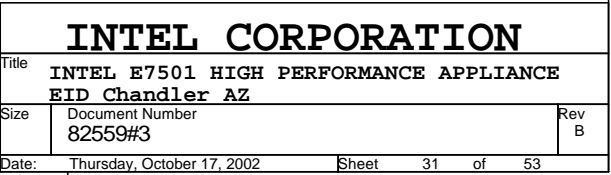


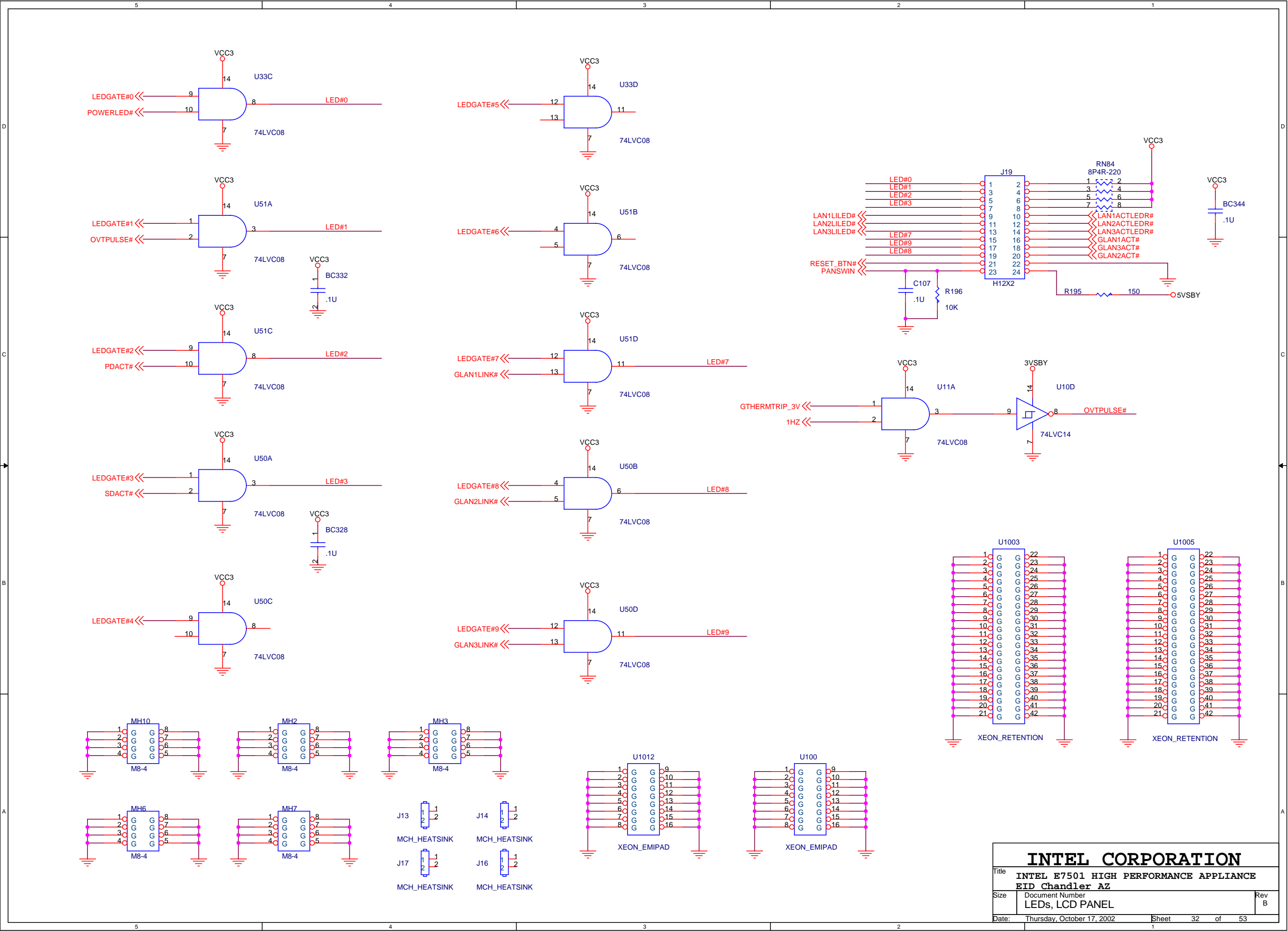


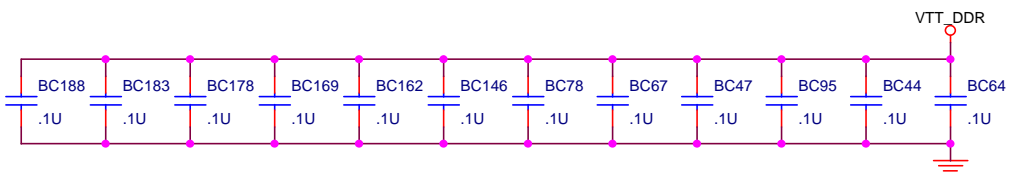


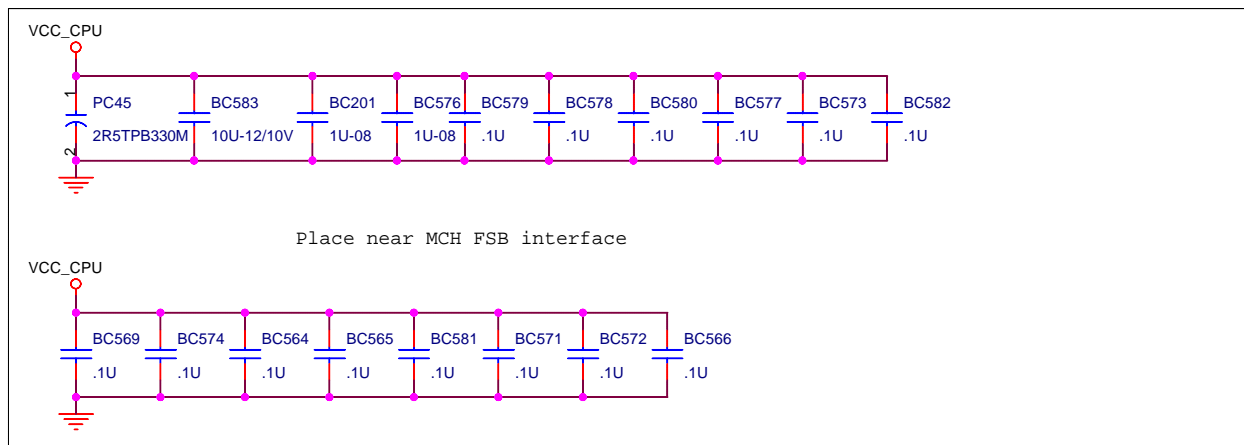
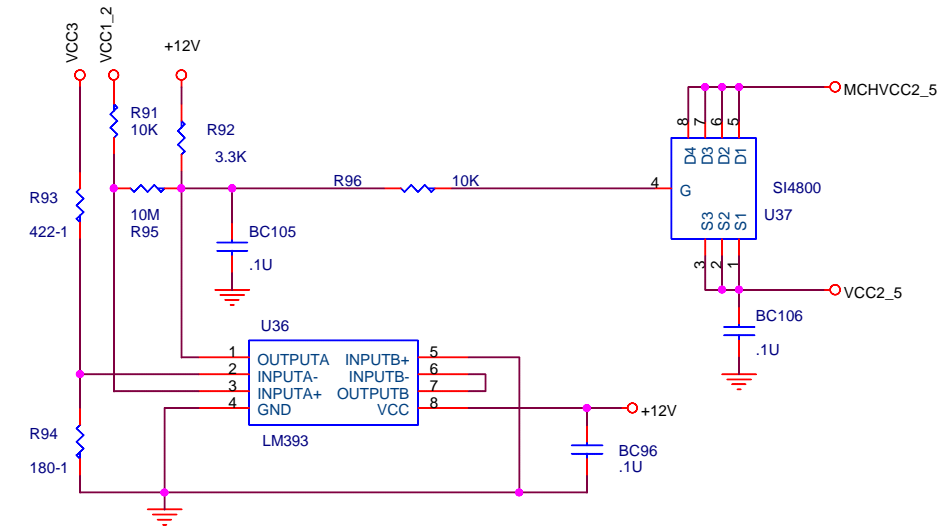


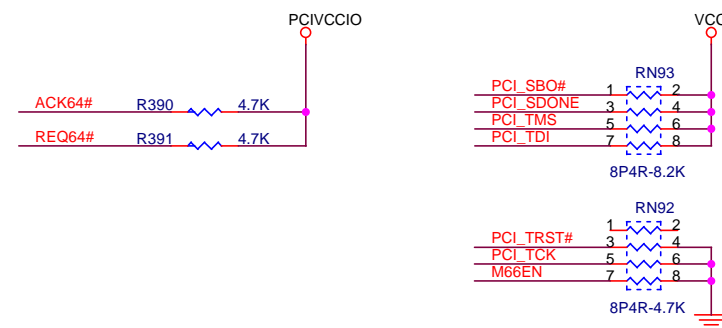
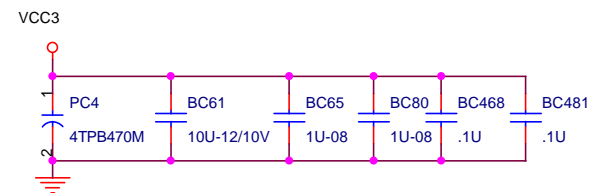
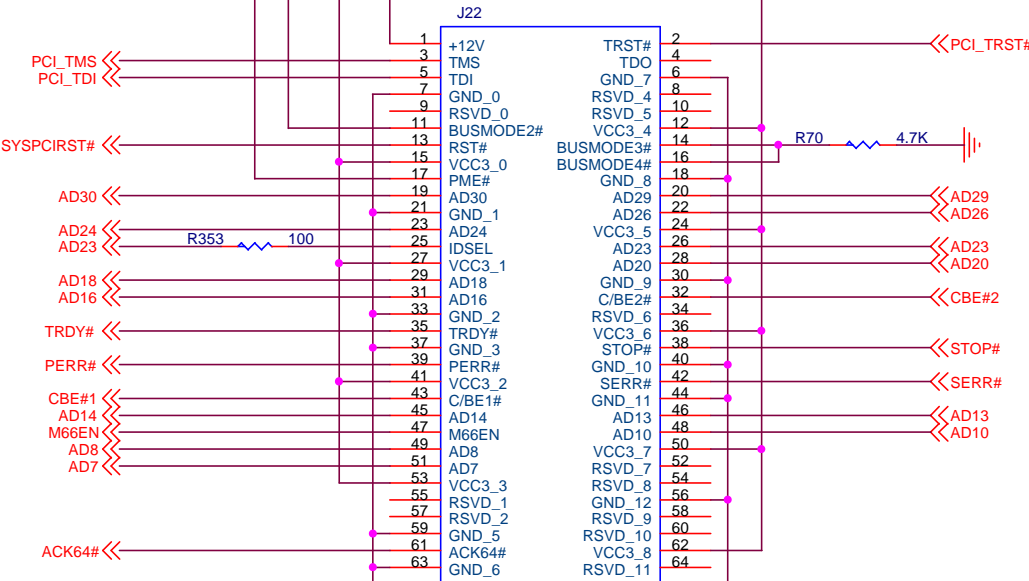
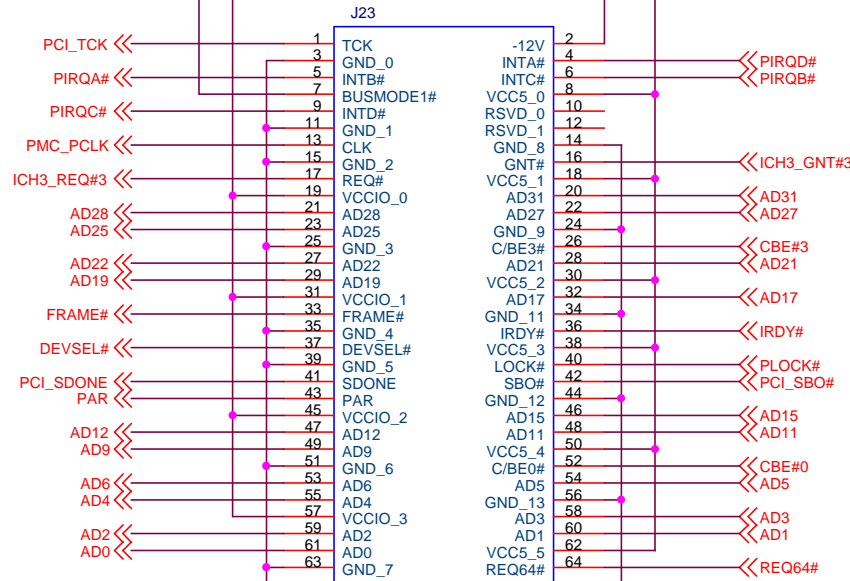


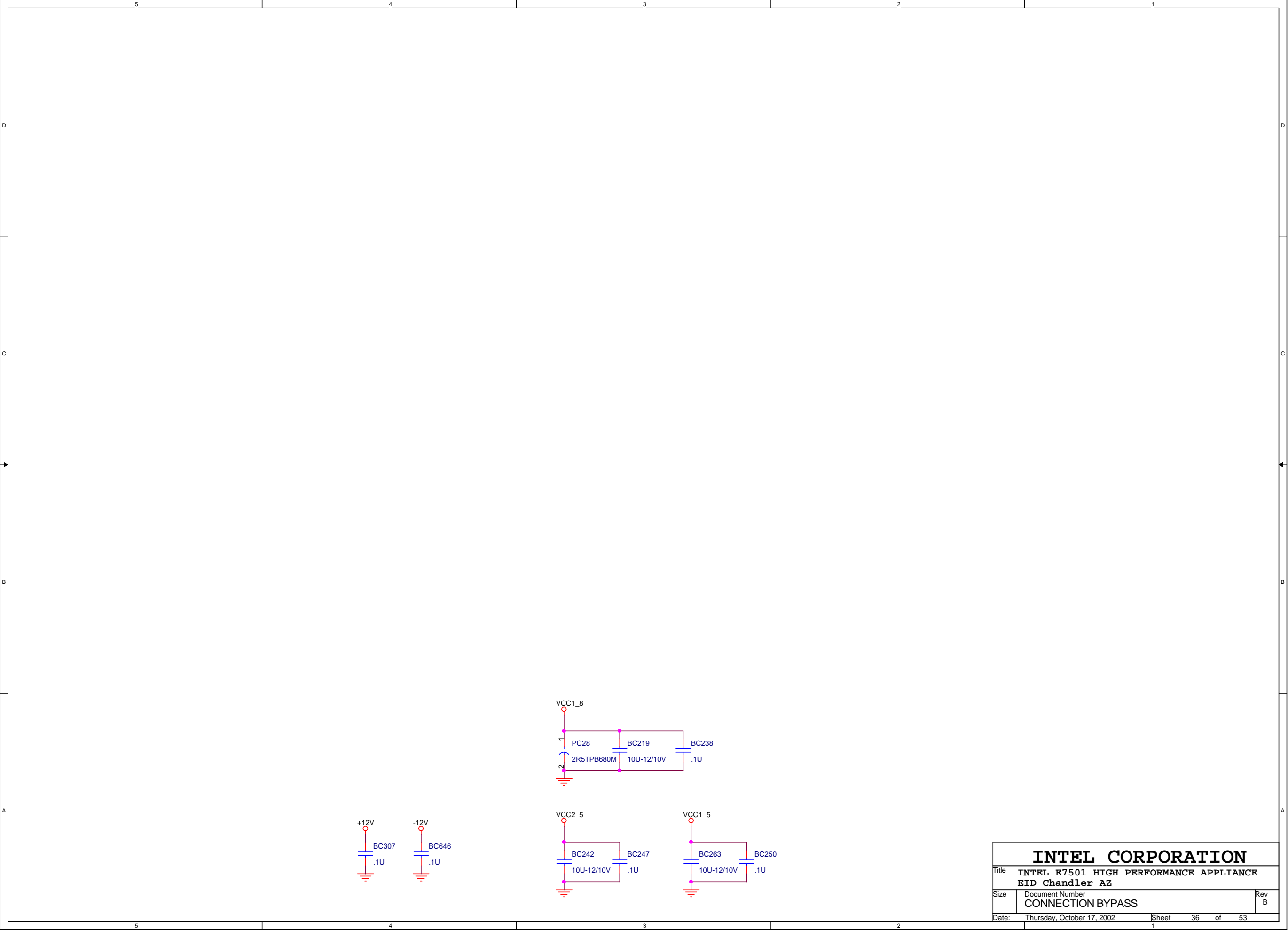




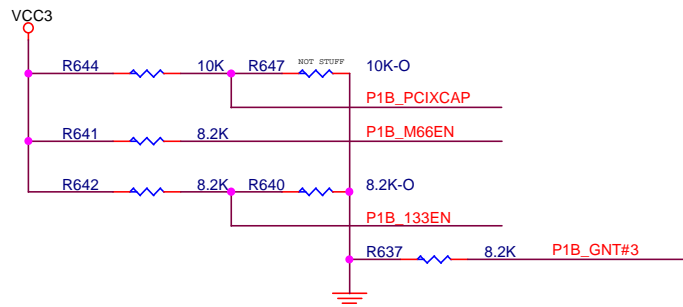
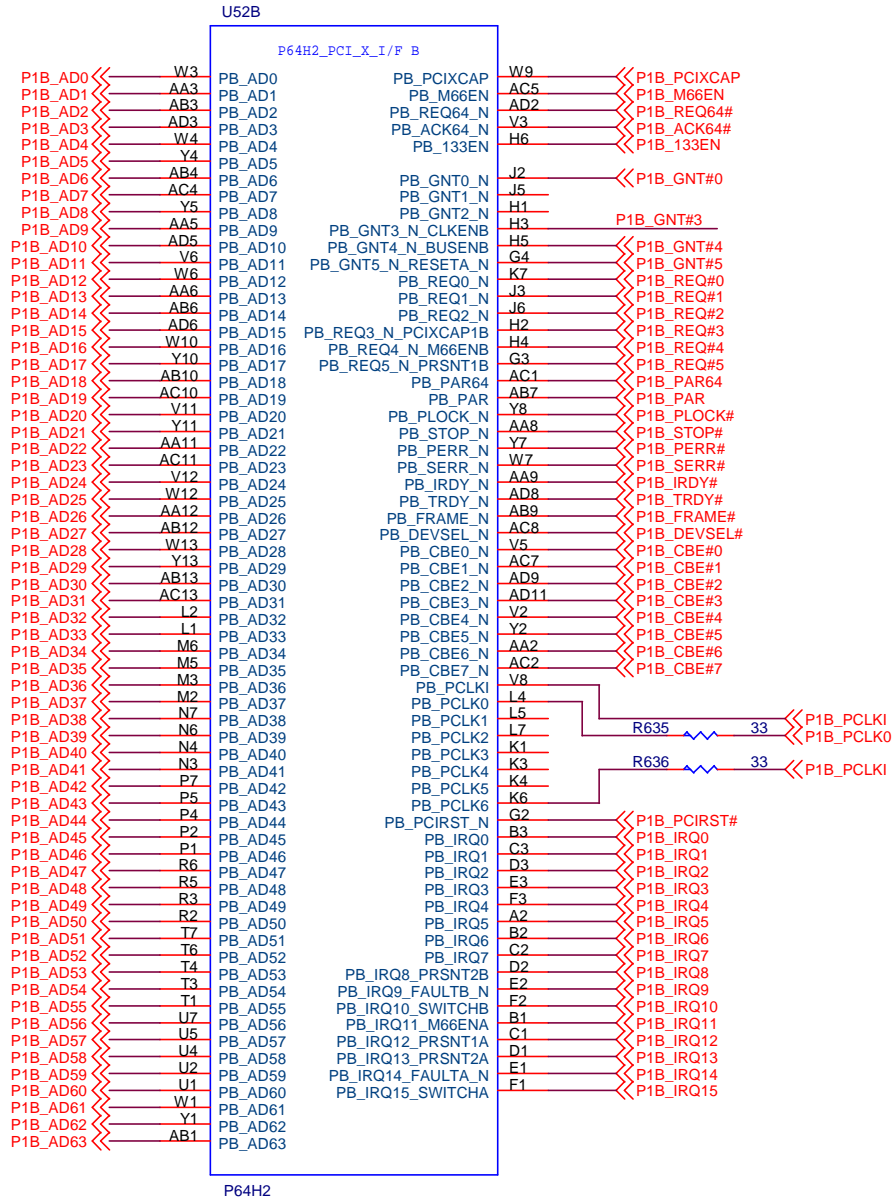
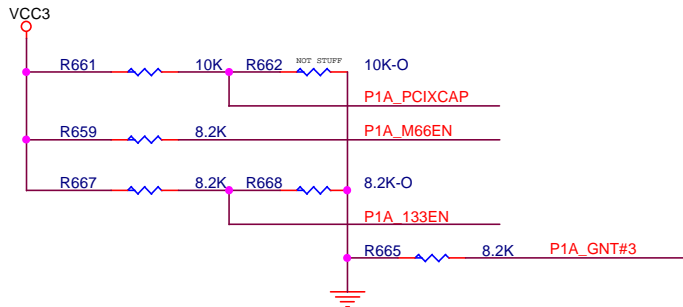
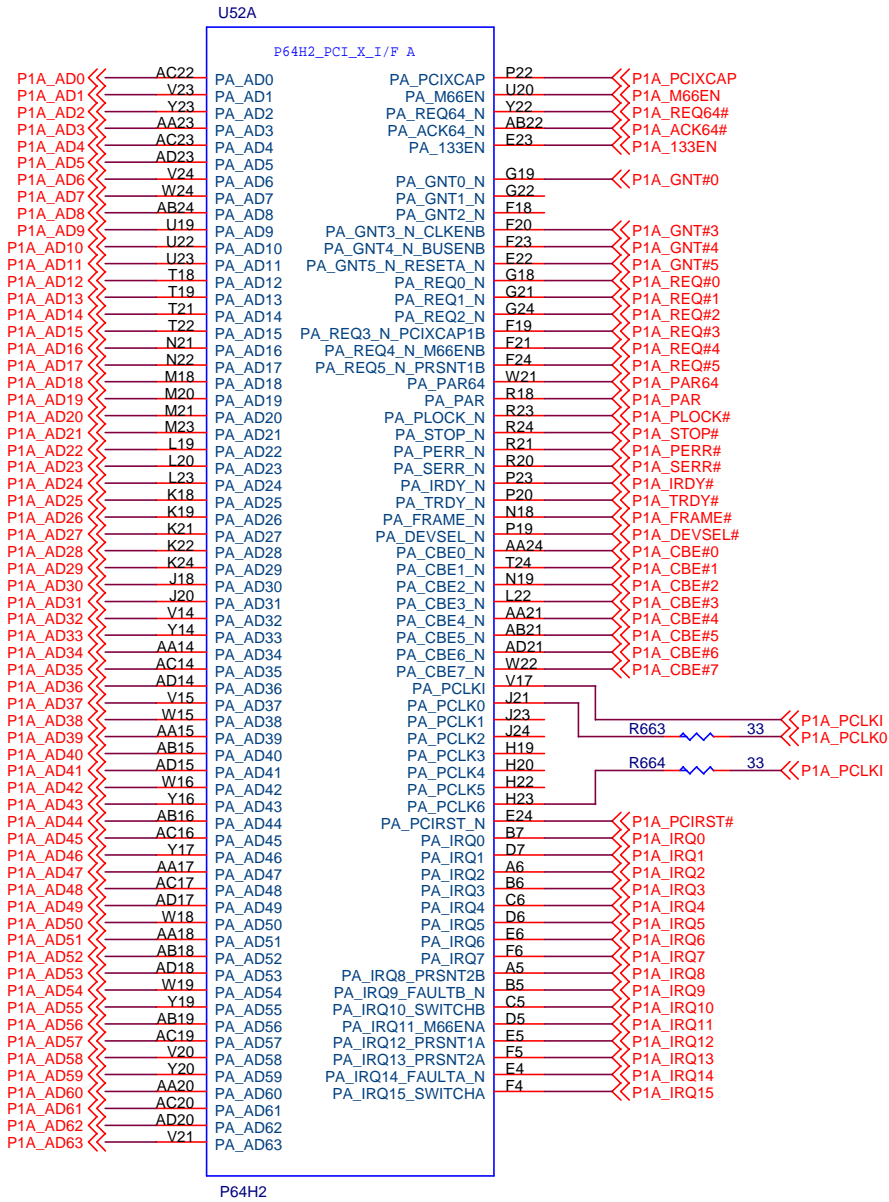


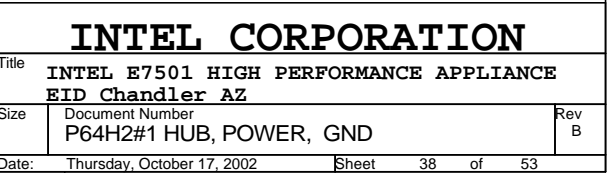


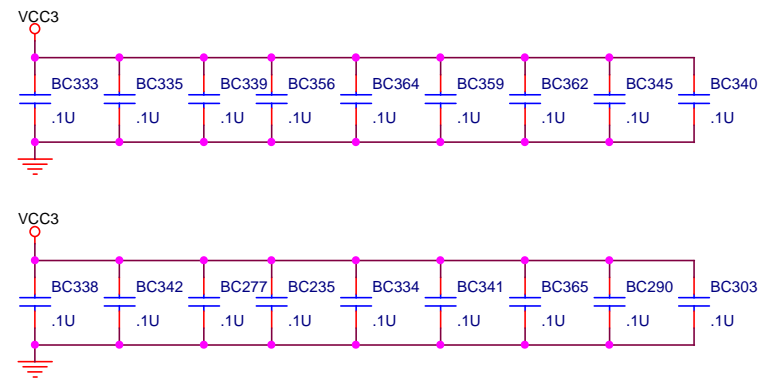
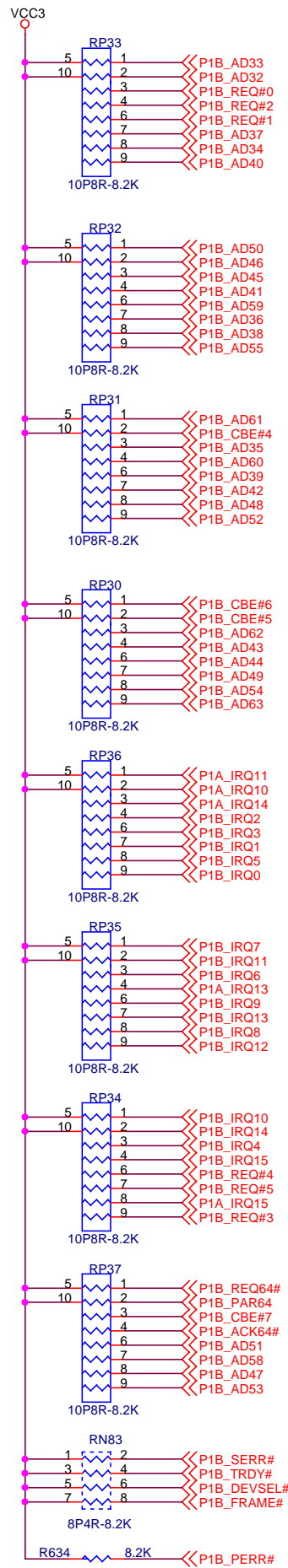
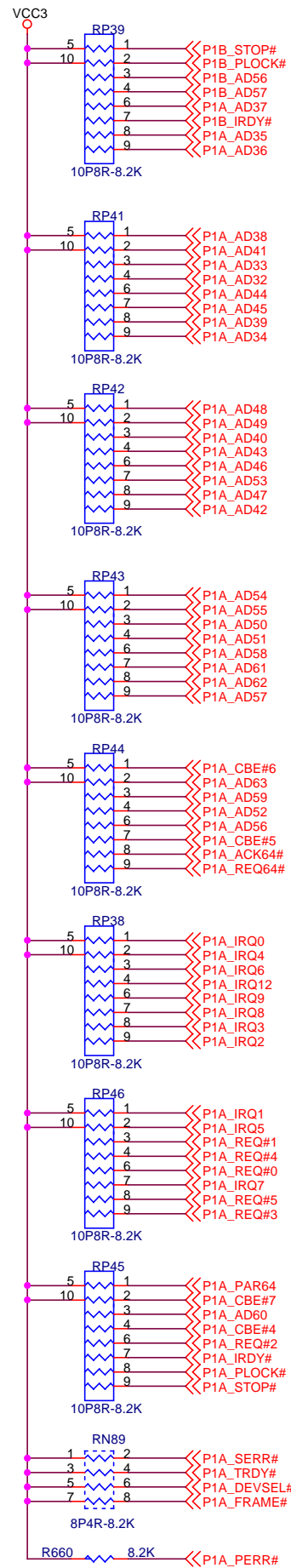


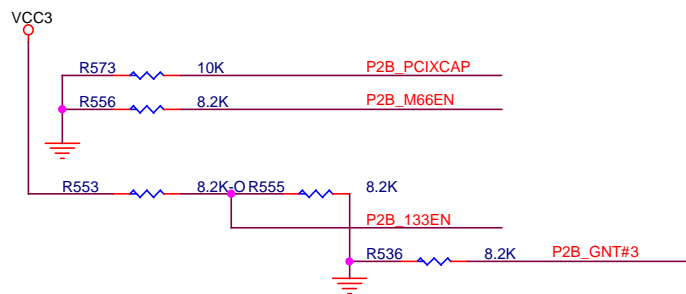
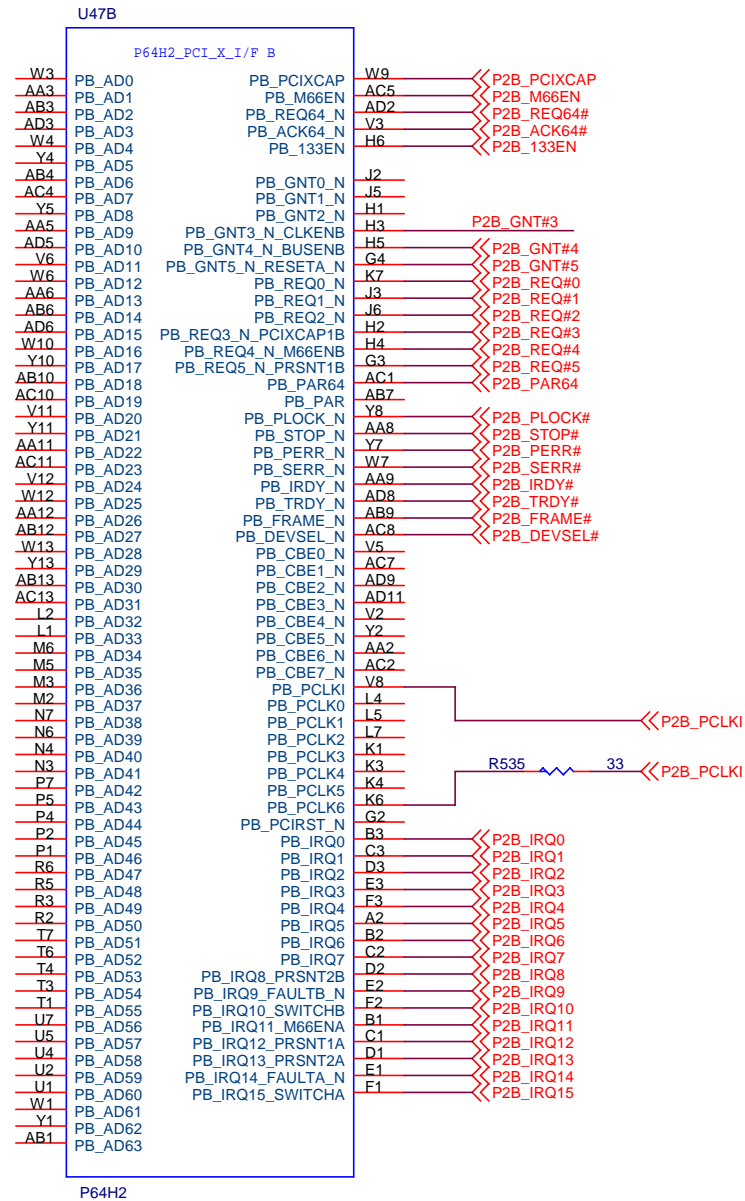
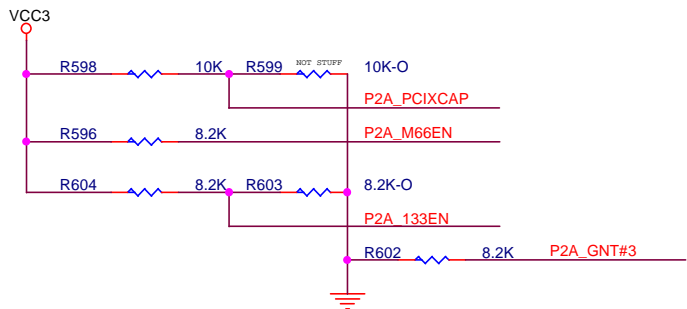
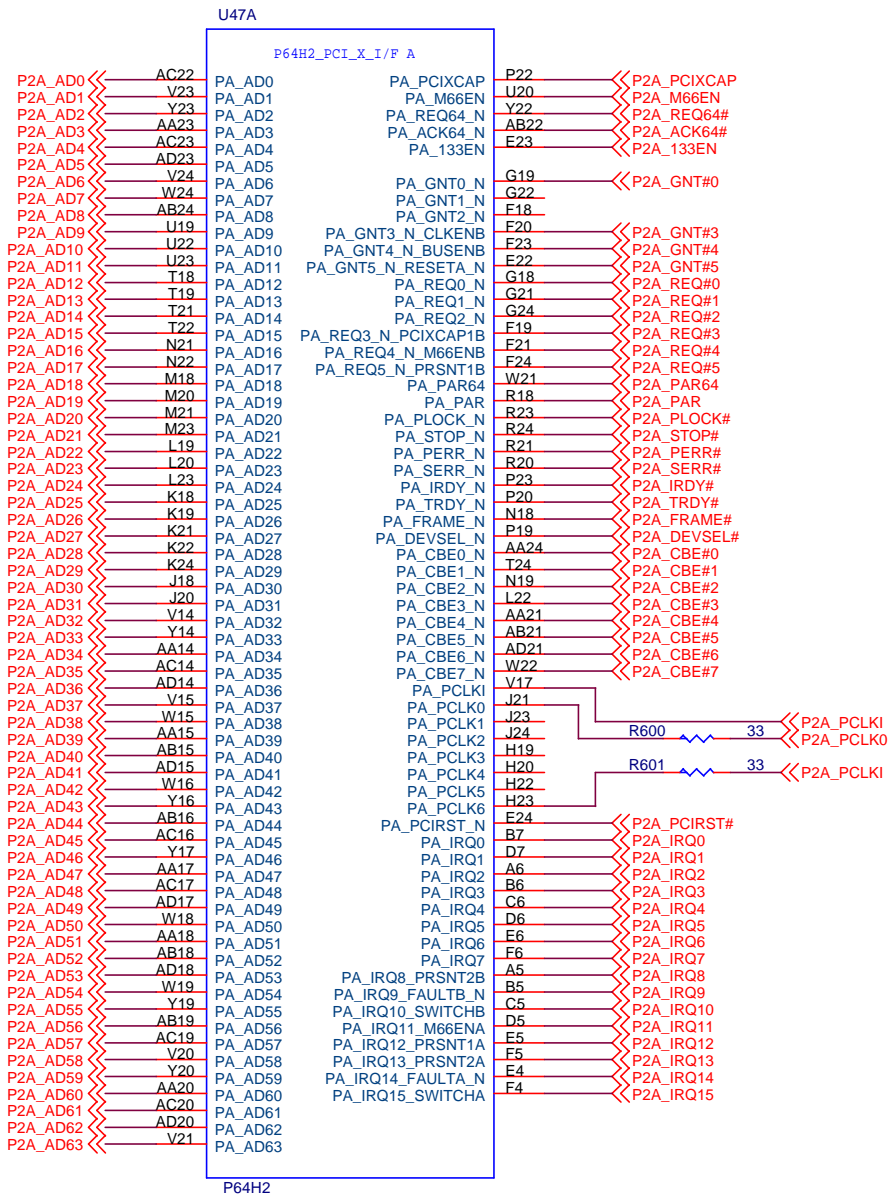


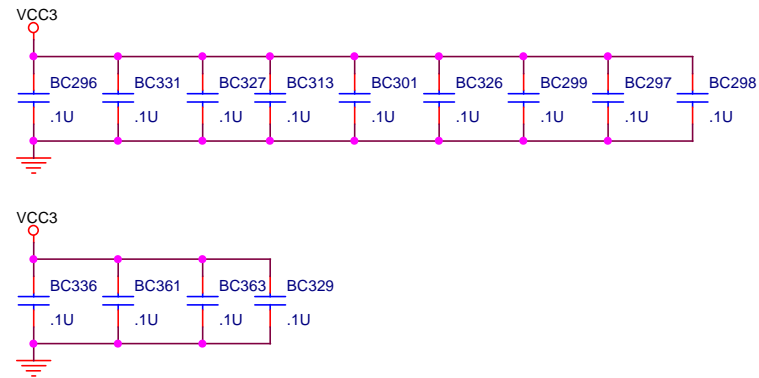
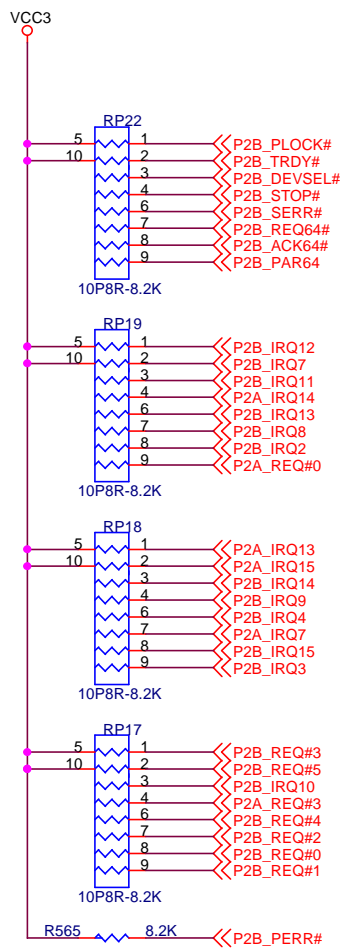
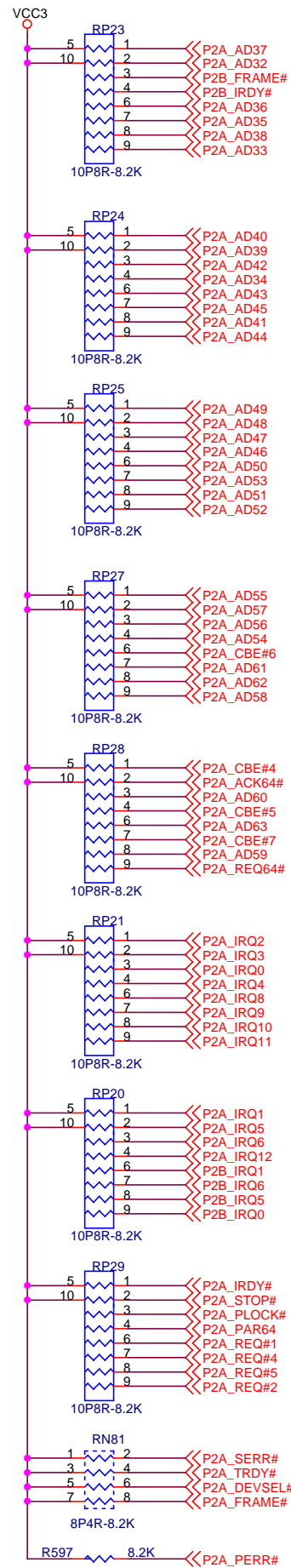
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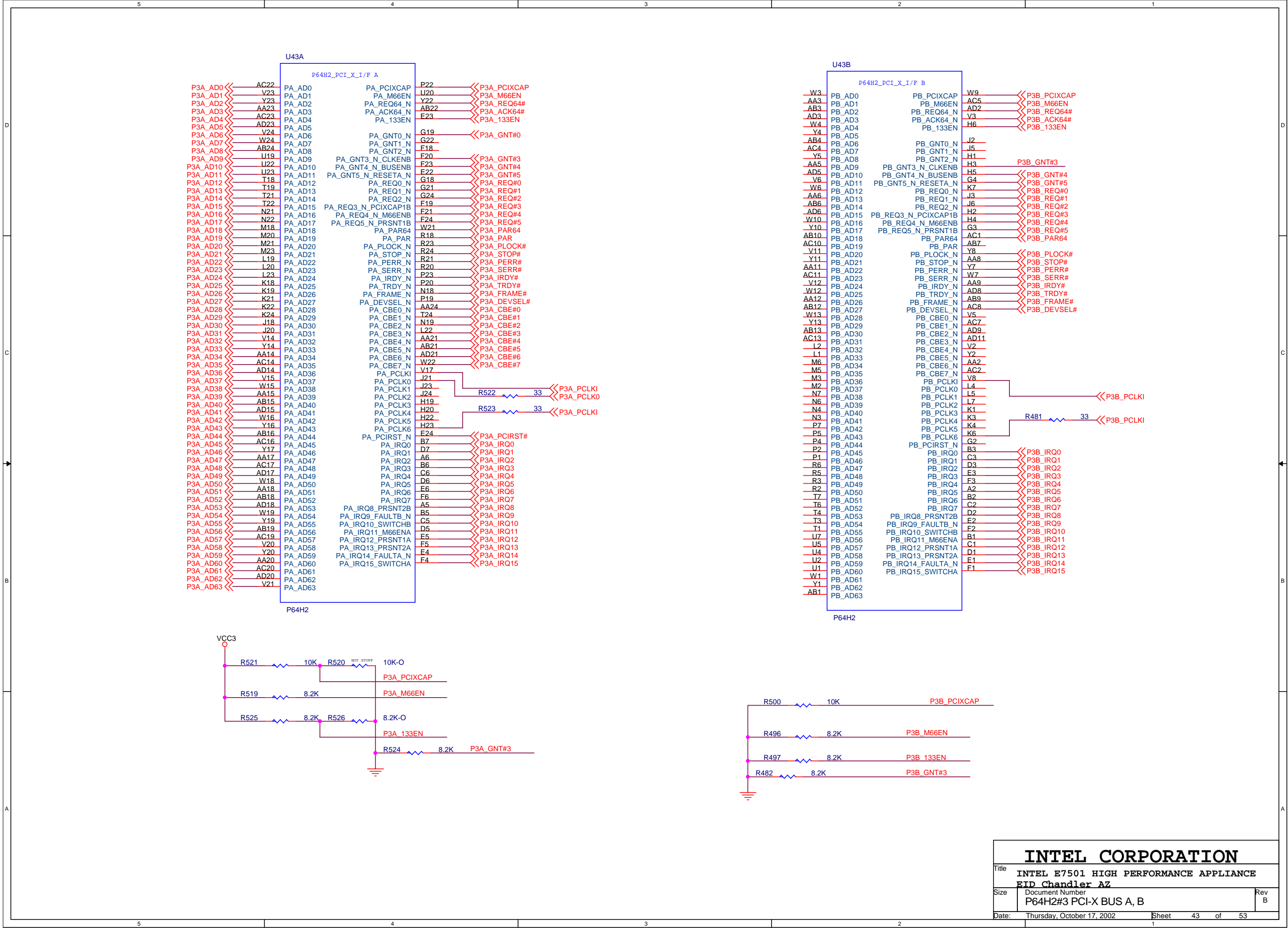


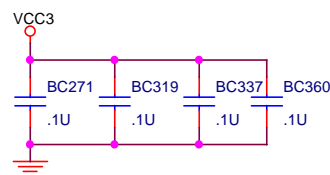
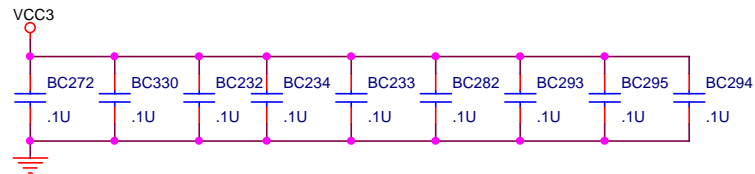
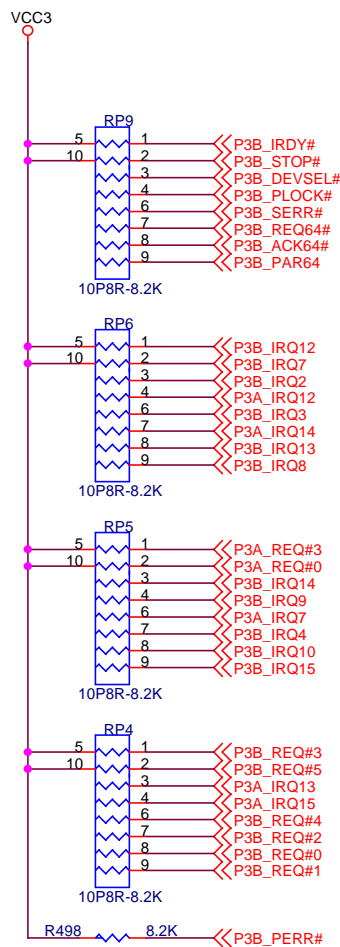
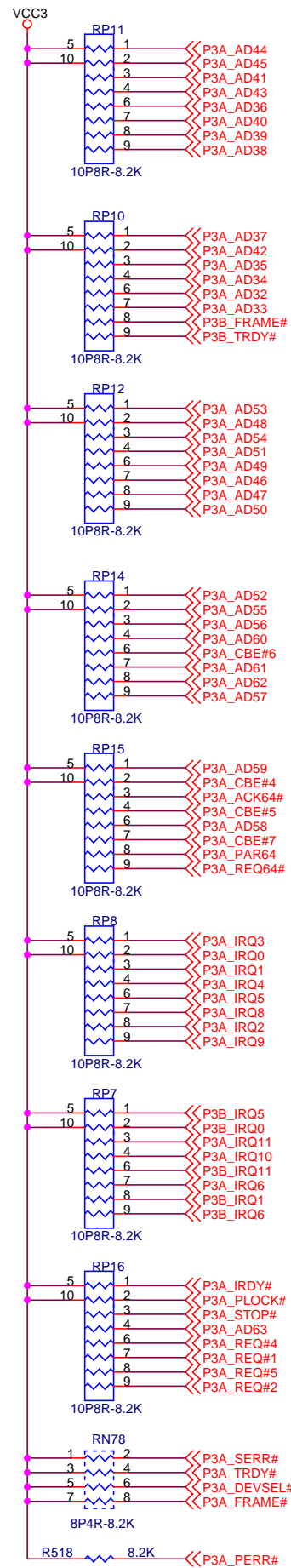




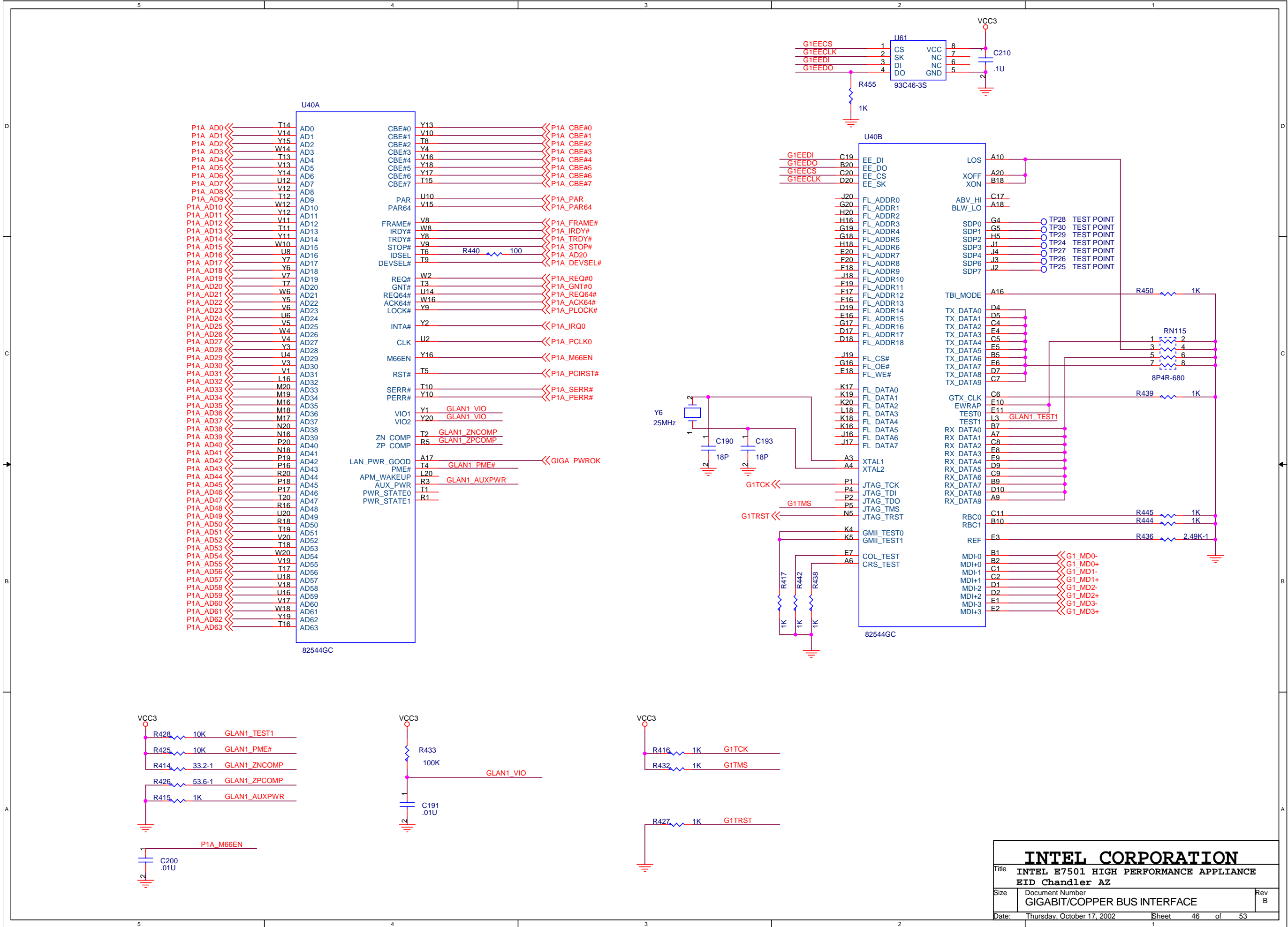


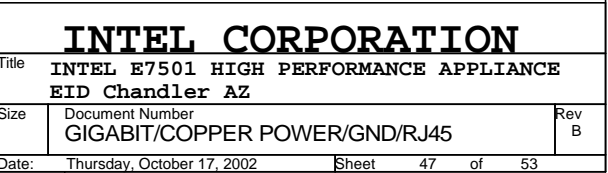


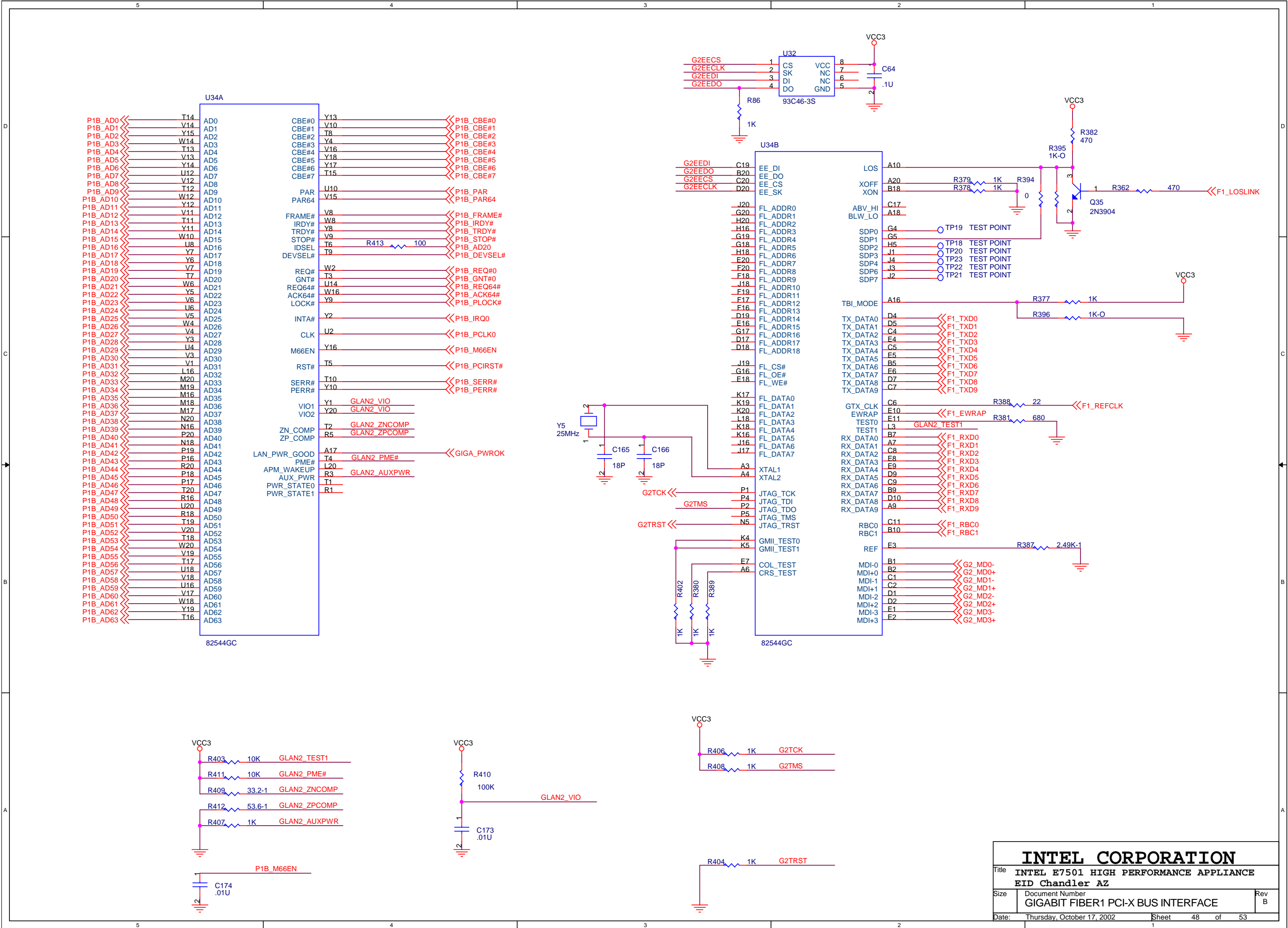




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